Analog Dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

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**ANALOG
DEVICES**

Editor's Notes

We first announced this Web Home Page almost exactly two years ago (Volume 29, No. 3, 1995). At that time, we bravely stated: "This site is intended to help engineers throughout the design-in process. There are articles and white papers discussing the underlying technologies, search tools to help you find the ideal component for your application, and we are developing a full set of material, including data sheets on every current part—and even SPICE models and evaluation-board layouts for many of them."
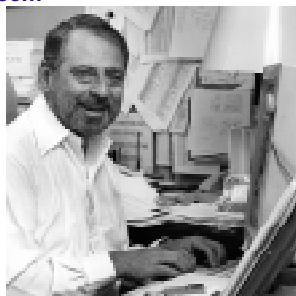
During the past two years, many of you have visited our Web site as it has developed. Some (hopefully, many) have been gratified, others (hopefully, few) have been disappointed. You've expressed your likes and dislikes quite volubly—*and we've been listening.* Other than personal contact with our sales and applications engineers, the Worldwide Web, through our site and our links with other sites, has become one of the most important ways of providing you with information—and hearing your feedback—truly another form of "Analog Dialogue".

We are in the midst of an immense work-in-progress to improve the user-friendliness, helpfulness, and intuitive nature of using the Web site throughout your design process—not just for product selection, but for support and procurement. Our objectives are: (1) continually earning your loyalty as a customer, (2) attracting more of your colleagues in the industry, and (3) achieving an interesting site with consistent, rapid, and complete content posting—one that you will want to visit frequently.

A few specific things we are seeking to improve are (1) speeding your ability to search the site and to use our search engines for comparative product selection; (2) increasing your ability to more easily become informed about "what's new" to the depth you need; (3) making easily available the information you need for making replacements, whether it be of competitive products you've been considering, or substitutions for obsolete ADI products; (4) speeding up the means of getting literature and samples to you; (5) making it easier for you to acquire catalog information; (6) increasing the ways to better interact with you in terms of improving feedback channels, answering applications questions, and making the features of our site that you regularly visit more readily accessible to you personally.

"Rome wasn't built in a day," but we think you will see visible signs of progress as the days go by in 1998. As always, your feedback is not only welcome—it's an essential part of the site's design. ▶

*Dan.Sheingold@analog.com*

IN THE LAST ISSUE

THE AUTHORS

Curt Ventola (page 3) is a Marketing Manager in ADI's Advanced Linear Products group, responsible for wired-communications line drivers, variable-gain amplifiers, and video encoders. He holds a BS in Material Engineering from Rutgers University and an MBA from Babson College. In his spare time, he enjoys racquetball, ice hockey, and coaching his sons' various sports teams.

Finbarr Moynihan (page 6) is a Systems Engineer with the Motion Control group, designing motor-control algorithms and specifying new single-chip solutions for motor control. He holds BE, M.Eng.Sc. (in EE) and Ph.D. degrees from University College, Cork, Ireland. His doctoral thesis was on applying DSP to motor control. He has authored papers and presented seminars on motion control theory and practice, and lectured in motion control at University College, Cork, and the University of Padova, Italy.

Paul Kettle (page 6) is a Senior Systems Engineer in the Motion Control group. His responsibilities include product definition and design-in opportunities in the Pacific rim countries, and software tool development strategy for the motion control group. He holds a Ph.D. in Stochastic Control and a B.Eng. in electronic engineering from Dublin City University. He has published widely on motion-control topics. Paul's main passion in life is sailing, and the sea in general.
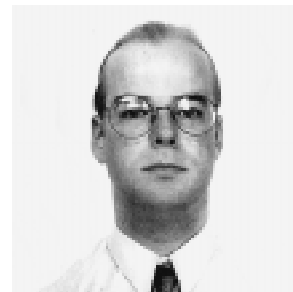
Tom Howe (page 6) is a Software Systems Engineer in the Motion Control group. He develops kernels, libraries, and software tools for motor-control DSPs. Tom has a BSEE from the University of New Hampshire and an MS in Computer Engineering from U. Mass., Lowell. In his spare time, Tom is renovating his house; he also enjoys reading, biking, and travel.

Cover: The cover illustration was designed and executed by **Shelley Miles**, of ***Design Encounters***, Hingham MA.

Analog Dialogue

Innovative Mixed-Signal Chipset Targets Hybrid-Fiber Coaxial Cable Modems

Jim Surber and Curt Ventola

The world is on the brink of a new era of widespread access to the information super highway, and cable modems are poised to provide the high-speed "on-ramp". Cable modems enable a CATV system with bidirectional hybrid-fiber coax (HFC) capability to serve as a two-way high-speed data port, which can be utilized to provide telephony and Internet access service to the home. Though a relatively small percentage of the US population is presently connected to the Internet, clearly its reputation as a valuable advertising and information resource is quickly spreading; the Internet is well on its way to becoming the backbone of the Information Age.

However, a roadblock to widespread adoption of the Internet is its painfully slow access time to PCs via the telephone modem. The slow response, and consequent user frustration, has slowed market growth and prevented the Internet from becoming an indispensable information tool for the average home consumer. The cable network industry has seen this as an opportunity to generate additional revenue by utilizing their vast cable plant resources, and 1-GHz network bandwidth, to provide higher-speed interactive data services to homes, institutions, and businesses. The major cable industry multi-system operators (MSOs) have announced their intentions to have cable modem service fully deployed by 1998.

As originally designed, the typical CATV cable plant was intended for one-way delivery of high-quality television signals to the home. The prospect of offering cable modems and other interactive video services has required the system owners to upgrade their plants by providing bidirectional signal capability. This has entailed the installation of a bidirectional hybrid-fiber coax trunk and 2-way line amplifiers. It is estimated that approximately 20% of the existing CATV plants have already been upgraded to full bidirectional capability. This would mean that some 20 million US homes and businesses could take advantage of bidirectional cable service.

What are the winning advantages of Internet access via cable modems and the CATV network over the prevailing telephone modem connection? First, the cable modem operates in a burst mode; this means that, while it remains physically connected to the cable plant, it only uses network resources when it transmits a burst of data. This allows the cable modem to be effectively always "signed on" to the Internet and ready for instant two-way data transfer. To accomplish this with a telephone modem would require a dedicated phone line—which leads to the next key advantage of cable modems: the cable modem does not tie up a phone line while the user is "surfing the 'net". With telephone modem access, unless there is a dedicated phone line, normal telephone service is suspended during Internet sessions.

Another advantage of cable modems is the dramatically increased speed of data delivery. Cable modems are capable of up to 36 Mb/s downstream data rates and 10 Mb/s upstream, compared to the standard telephone modem service of 28 kb/s up and downstream (56 kb/s max). This many-fold increase in data-transmission speed means that the Internet access speed will be generally limited by URL file servers rather than the modem baud rate. This is especially important when the user is downloading large graphic, video, or image files. A file that takes 8 minutes to download via a 28.8-kb/s telephone modem takes 8 seconds via cable modem. This increased access speed will unleash the true power of the Internet's imaging potential.
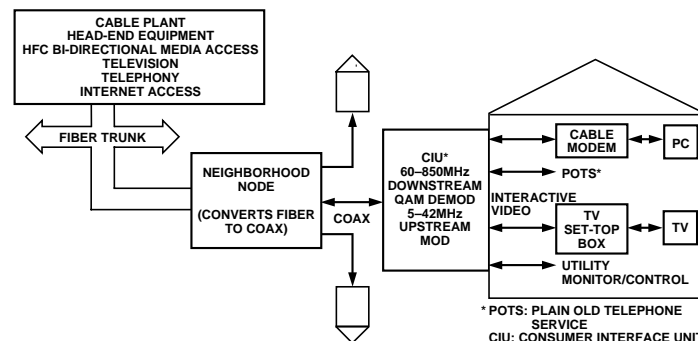
Figure 1. Block diagram of HFC CATV plant.

The cable industry would prefer that cable modems for Internet surfing become "off-the-shelf" items, purchased and maintained by the consumer, very much like telephone modems. To this end, cable modems would need to be interoperable, which means that a given cable modem will work in different cable systems, with different-vendors' head-end equipment. To achieve interoperability of cable modems, universal standards are required—and indeed, they are emerging. The Multimedia Cable Network Systems (MCNS) group has issued their "Data over cable services interface specifications" for interactive communications via the HFC network. The MCNS standards have been endorsed by many of the larger cable MSOs as their working standard. The IEEE 802.14 committee is also developing a set of standards for HFC cable networks, and the DAVIC and DVB standards have been released and are being deployed in Europe. For cable telephony, however, proprietary algorithms are employed for upstream/downstream transmissions, and interoperability is not a concern.

The basic cable modem consists of an RF receiver and transmitter physical layer, the PHY, that modulates/demodulates the data, and

a media access controller, the MAC, that performs the master system control function. When the standards are fully deployed, the downstream data delivery will take place in the 42-850 MHz band with existing 6-MHz CATV network channel spacing. The downstream digital modulation format will be 64-QAM (quadrature amplitude modulation), with a future migration to 256-QAM. The HFC data delivery system will be asymmetric; the data rate will be faster downstream than upstream. This is generally compatible with Internet surfing applications, since typical http navigation calls for much more data to be sent down to the computer than up to the network.

The upstream transmit path, required when using cable modems, is the major new requirement that has been placed on the CATV plant. The bandwidth that has been allocated for the return-path function by the cable industries is 5-42 MHz in the USA, and 5-65 MHz in Europe. This particular bandwidth is expected to contain substantial amounts of impulse noise, or "ingress", which will make reverse path communication difficult. Initially, a relatively simple modulation format, quadrature phase-shift keying (QPSK), is being utilized by most cable modem vendors. In the future, as the cable plant environment is further upgraded and improved, there will be a movement to a 16-QAM upstream modulation format to increase the bits/Hz efficiency of the upstream data transmission.

Some of the technologically and market-driven requirements for the upstream transmitter (Tx) section of a cable modem are:
• Output frequency agility with digital control
• Full digital control of modulation and output power parameters
• High spurious-free dynamic range (SFDR) on the modulated output carrier
• Integrated digital signal processing with a high level of functionality
• Low cost
• Low power

Analog Devices is in a unique position to supply an optimum silicon solution for the upstream Tx requirement; it falls squarely in the domain of ADI's mixed-signal and linear core competencies. The AD9853/AD8320 upstream-Tx chipset*, available now, integrates the high-speed digital and analog blocks that provide a complete ASIC solution for the HFC upstream transmitter requirement. The AD9853 is a modulator function that has been specifically defined to meet the requirements of both interoperable and proprietary implementations of the HFC upstream function. The

AD8320 is a companion cable driver amplifier, with a digitally programmable gain function; matched to the output of the AD9853 modulator, it directly drives the cable plant with the modulated carrier. Together, the AD9853 and AD8320 fully meet the HFC return-path requirement.

The AD9853 CMOS digital modulator combines high-speed conversion, direct digital synthesis, and digital signal processing technologies. The modulator architecture is digital throughout, which provides definite advantages in I/Q channel phase- and amplitude matching, and long-term modulator stability. The AD9853 is programmed and controlled via a serial control bus that is I²C compatible. The basic modulator block consists of an input channel encoder which formats the input data stream into the desired bit-mapped constellation and modulation format. The data stream is demultiplexed into I/Q channel data paths that are individually FIR-filtered to provide the desired pulse response characteristic for controlled output burst ramping. Then interpolating filter stages are used to match the effective output data rate of the FIR filters to the output sampling frequency of the direct digital synthesizer (DDS) for frequency upconversion.

The AD9853 employs a state-of-the-art DDS function to generate precise sine and cosine digital waveforms to mix with the pulse-shaped data bitstream in a high-speed mixer stage, and create the 5-42 MHz modulated carrier. The DDS is also responsible for making the device highly frequency-agile; its 32-bit tuning word capability enables the modulated carrier at the output to be tuned with a resolution of 0.029 Hz.

A high-speed adder stage sums the upconverted digital I and Q data to create a single data path, which is ready to be converted into the analog domain by a high-speed 10-bit D/A converter. A SINC filter is utilized to "pre-compensate" the data stream for the sinx/x roll-off of a high-speed D/A converter's quantized output function. The patented architecture of the AD9853's CMOS D/A converter stage, with a 55-dB SFDR at 40 MHz Aout, rivals the performance afforded by expensive and power-hungry bipolar DACs.

A key system cost-saving feature in the AD9853 is its ×6 reference-clock multiplier circuitry, which essentially allows the AD9853 to generate the high-speed clock for the DDS synthesizer internally, saving the user the expense and system design difficulty of

*For technical data, consult our Web site, **www.analog.com**, use Faxback to request **2169/2203** (see page 24), or use the reply card: **circle 1**
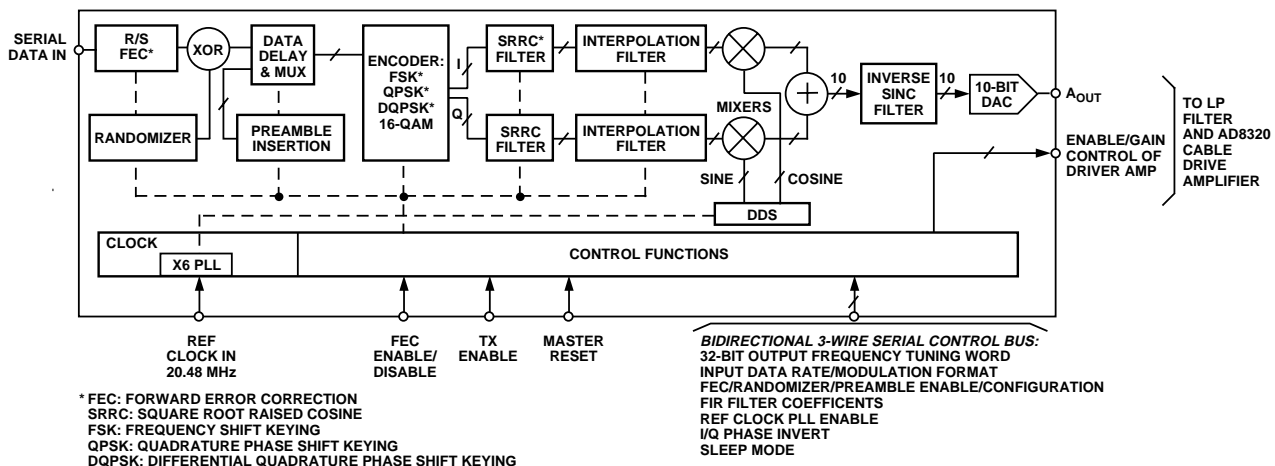

Figure 2. AD9853 digital modulator block diagram.

implementing an external 122-MHz reference clock (160-MHz clock for 65-MHz carrier applications). The SFDR specification is achieved with the low-jitter clock multiplier circuitry enabled.

Additional programmable functions that support the requirements of HFC 2-way communication applications include forward error correction, data scrambling, and preamble word insertion. These are functions specified for successful burst packet data transmission in interoperable implementations of cable modems. The AD9853 also includes an output serial-data control function for interfacing directly to the AD8320 cable-driver amplifier. This control function allows the AD9853 to enable the AD8320 automatically at the appropriate time in a burst transmission sequence and allows the cable modem's MAC function to control the output power of the modem via the AD9853's control bus.

The AD9853 modulator output is connected to the input of the AD8320 programmable cable driver amplifier through an external low-pass filter, which is necessary to suppress the aliased images that are generated by the DAC's sampled output. The first aliased image occurs at $F_{sampling} - F_{out}$, which necessitates a fairly sharp-cutoff low-pass filter function. An inexpensive 7-pole elliptical low-pass passive 75-ohm LC filter can be implemented between the AD9853 and AD8320 to suppress the output aliases sufficiently for the HFC network application.
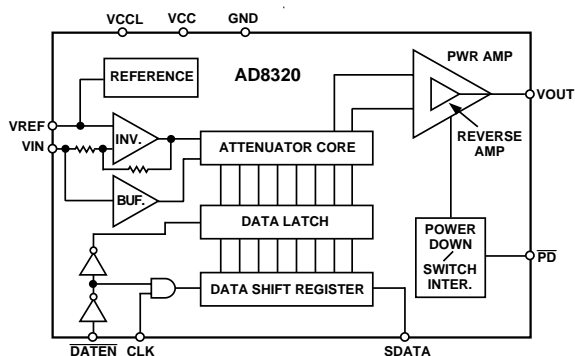

Figure 3. Block diagram of AD8320 digitally programmable cable-driver amplifier.

The AD8320 is a digitally-programmable cable driver amplifier (using a bipolar IC process) that directly interfaces to the 75-Ω cable plant. It provides 36 dB of programmable gain range with a maximum power output level >18 dBm (6.2 V) into a 75-Ω load. The gain of the AD8320 is controlled via an 8-bit SPI serial control word. The AD8320 accomplishes programmable gain control with a bank of 8 binary weighted transconductance (g_m) stages, which are connected in parallel to their respective load resistors. The total attenuation of the core is determined by the combination of g_m stages selected by the data latch. The eight g_m stages, with their 256 levels of attenuation, provide a linear gain function with a dynamic range of 36 dB ($\cong$64 V/V full scale).

The AD8320's harmonic distortion is typically –57.2 dB for a 42-MHz output and –54 dB for 65-MHz output, at an output power level of 12 dBm into 75 Ω. This dynamic performance supports the requirements of cable telephony and data services over the HFC network. The AD8320's output stage has a dynamic output impedance of 75 Ω. This allows for direct single-ended connection of the device output to the CATV plant without back-termination, retaining the 6 dBm of load power that would be lost using the 75-Ω back-termination resistor required by the traditional low-output-Z driver amplifier. In fact, the AD8320 maintains

75-Ω impedance at its output during device power down to minimize glitches during transitions. This helps minimize line reflections and insures proper filter operation for any forward mode device sharing the cable connection. Another advantage of the dynamic 75-Ω output impedance is that it saves cost significantly by eliminating an expensive GaAs switch, which would otherwise be required to minimize transitional glitches.
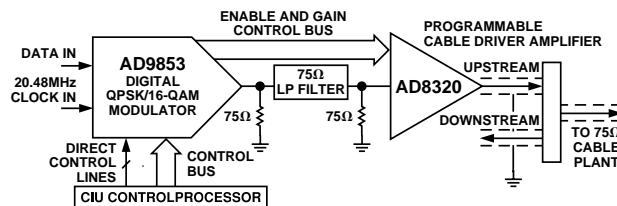
Figure 4. AD9853 and AD8320 in upstream Tx application.

The AD9853/AD8320 chipset combination offers the highest dynamic performance available from an integrated chipset for the HFC upstream Tx function. As Figure 5a shows, the chipset will typically deliver a signal to the cable plant's diplexer filter with >50 dB spur rejection for a 42-MHz 16-QAM-modulated carrier. Figures 5b & c show a typical eye diagram and constellation for a 16-QAM modulated carrier; the chipset delivers error-voltage magnitude (EVM) performance of <2%. I/Q phase imbalance is typically less than 1°, due to the all-digital modulator scheme. Evaluation is facilitated by available board, the AD9853-45PCB, which includes AD9853, AD8320, and a 45-MHz LP filter.
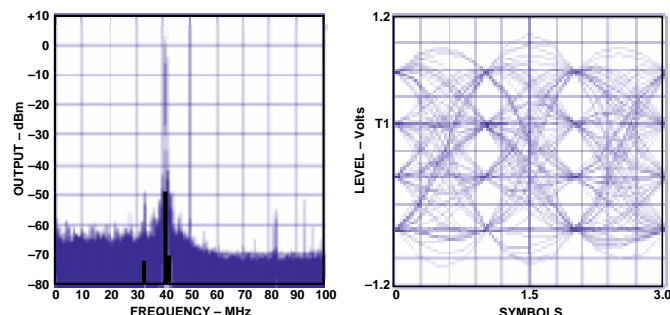
a. Output spectral plot.

b. Eye diagram.
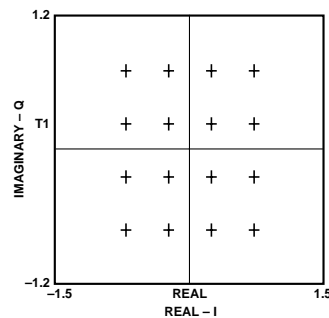
c. 16-QAM constellation.

Figure 5. AD9853/AD8320 chipset performance with 42-MHz carrier 16-QAM-modulated @ 320 ksym/s.

To summarize, the upstream transmitting chipset, with its high level of functional integration and state-of-the-art mixed-signal technology, today offers an effective silicon solution for the two-way HFC network, to help usher in the next wave of information resources for the home consumer. Developments to look forward to include compact downstream tuners and demodulators, and—ultimately—a single-chip complete cable modem solution. ▶

Powerful Design Tools for Motion Control Applications

Finbarr Moynihan, Paul Kettle,
Aengus Murray, and Tom Howe

Introduction

The need for sophisticated solutions for motor control continues to increase in the consumer, appliance, industrial and automotive markets. A wide variety of motor types are in use, depending on the application; the most common include the ac induction motor, permanent-magnet synchronous motor, brushless dc motor and such newer designs as the switched-reluctance motor. Indeed, many applications, which were formerly dominated by constant speed, mains-fed induction motors, now require the sophistication of variable speed control. In some applications, such as compressors, fans and pumps, this need for increased sophistication is driven by legislation and consumer demand for higher operating efficiencies. Elsewhere, high-performance applications in process control, robotics and machine tools demand variable speed and increased precision, achievable only by the use of sophisticated control algorithms.

The key to the real-time implementation of sophisticated control algorithms for these motion control systems has been the advent of powerful digital signal processors (DSPs).* Even in less-demanding—but cost-sensitive—applications, such as domestic refrigerator compressor drives, the power of the DSP can be harnessed to implement sensorless control algorithms that reduce the system cost and increase the overall robustness of the drive. In high-performance servo drives, the powerful computational ability of the DSP permits more precise control through vector control, ripple torque reduction, predictive control structures, and compensation for non-ideal system behavior.

Besides the powerful DSP core, all motor control systems require a significant array of additional circuits for correct operation, including such functions as:

- Analog-to-digital conversion for current or voltage feedback
- Pulsewidth modulation (PWM) blocks for generation of the inverter switching commands
- Position-sensor interfaces for higher-performance applications
- Serial ports for host communications
- General purpose digital input/output ports.

Analog Devices now offers a range of *single-chip* DSP-based motor control solutions that integrate these peripheral functions with a high performance DSP core and the required memory. Two devices are described here: the ADMC330†, designed for low-to-medium performance dynamic requirements, and the ADMC300†, which extends the single-chip capability to control of high-performance servo drives.

ADMC330 Single Chip DSP-Based Motor Controller (see Figure 1): The ADMC330 integrates a 20 MIPS DSP core, 2Kword program memory RAM, 2Kword program memory ROM, 1Kword data memory RAM, 2 serial ports and a variety of motor-control peripherals onto a single chip. The DSP core is similar to that used in the 16-bit fixed-point ADSP-2171. The motor control peripherals include 7 analog inputs with a comparator based ADC subsystem that permits 4 conversions per PWM period. In addition, a sophisticated 3-phase, 12-bit, PWM system enables all necessary inverter switching signals to be generated, timed to within 100 ns, with minimal processor overhead. Dead-time of these PWM signals may be adjusted in the processor so that no external logic is required. The PWM unit includes special modes for brushless dc motors or electronically commutated motors, where only two of the three motor phases conduct at the same time. In addition, the ADMC330 includes 8 digital I/O lines, a watchdog timer, a general purpose 16-bit timer and two auxiliary PWM outputs.

ADMC300 Single Chip DSP-Based Servo Motor Controller (Figure 2): High-performance servo drives, for robotics and machine tools, require high resolution ADCs and a position sensor interface to meet the demanding performance requirements. The ADMC300 addresses these needs in a single-chip DSP-based solution for these applications. The ADMC300's additional functionality for more-demanding applications includes a DSP core enhanced for 25-MIPS performance. In addition, the program memory RAM has been doubled to 4K words. The need for multichannel, high-resolution ADCs is met by including five independent sigma-delta ADCs that provide 12 bits of resolution. Analog signal expansion is made possible by the provision of three external multiplexer control lines. In addition, the ADMC300 facilitates position sensing via an encoder interface that allows easy connection to an incremental encoder.

Development Tools: Since software is the key to the use of digital equipment, powerful processing capability requires an equally powerful development system in order to use these sophisticated motor controllers in real applications. Both processors come with

*See "Motion Control Chip Sets" in *Analog Dialogue* 30-2 (1996), pp. 3-5.
†For technical data, consult our Web site, **www.analog.com**, use Faxback to request **2126 and 2253** (see page 24), or use the reply card: **circle 2**
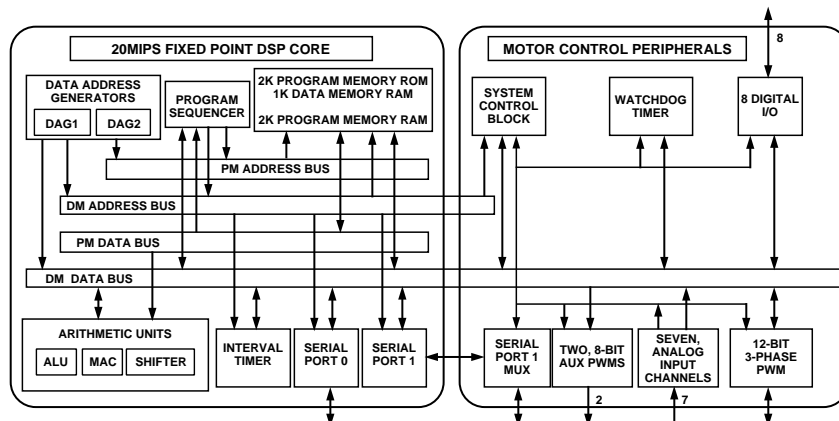

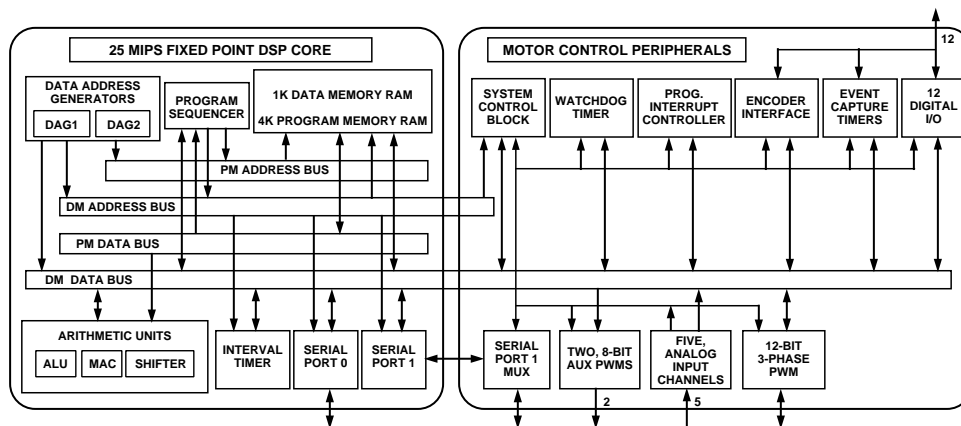Figure 1. The ADMC330 single-chip DSP-based motor controller.

Figure 2. The ADMC300 Single-Chip DSP-based Servo Motor Controller.

a full range of hardware and software development tools that allow rapid prototype development and real system evaluation. In both the ADMC300 and the ADMC330, the program-memory ROM block is preprogrammed with a monitor/debugger function that enables access to the internal registers and memory of the processors. In order to speed program development, the ROM code also contains a library of useful mathematical and motor-control utilities that may be called from the user code.

A separate evaluation board for code development is available for each type. These evaluation boards contain easy interfaces to the many peripheral functions of the processors, so that the board can be easily integrated into a final target development system. Each evaluation board contains a UART interface that may be used to connect the DSP controller to a Windows-based Motion Control Debugger program. The debugger program allows the developer to download code to the DSP and monitor or modify the contents of program memory, data memory, DSP registers, and the peripheral registers. In addition, a selection of debugging tools— including breakpoints, single-step, and continuous-run operation— may be selected from the Windows menu. The sample screen from the ADMC330 debugger shown in Figure 3 illustrates many of the features of the debugger. Additional software tools—such as the assembler, linker, and PROM programmer—are also included. For stand-alone operation, the evaluation boards may also use external memory for boot program loading.
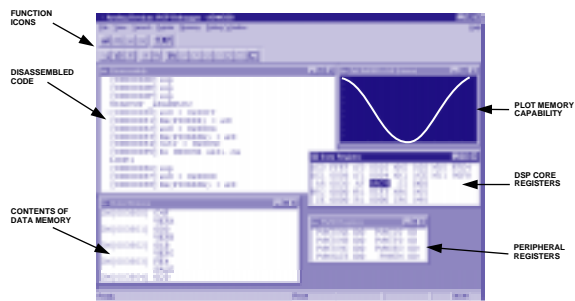

Figure 3. Sample Output Screen of Motion Control Debugger for ADMC330.

ADvanced Pow_IR_train™: In order to develop real motor-control solutions, the computing power of the DSP must be combined with a suitable power-electronic converter that produces the required voltages to drive the motor in response to the control commands (and can furnish the necessary currents). The ADvanced Pow_IR_train board represents a new departure in development systems for real world motor control systems. The board integrates Analog Devices's high-performance DSP-based motor controllers with an appropriate International Rectifier

[www.irf.com] Pow_IR_train™* integrated power module; it provides all of the necessary circuitry to permit development of motor control algorithms for a variety of applications. Using plug-in interchangeable processor modules, the user can choose the level of control appropriate for the application.

With the ADMC330 processor module, the board may be used to develop sensorless control algorithms for brushless dc motors for applications such as compressors and washing machines. In addition, simple vector-control strategies for an ac induction motor may be programmed for pump or fan applications. If higher performance levels are required, the ADMC300 processor module may be mounted instead, to implement open-loop and closed-loop vector control of induction motors, for applications such as general-purpose variable speed drives, paper and textile machines, and conveyors. With the ADMC300 processor module, the ADvanced Pow_IR_train is suitable for developing high-performance servo controllers using an induction motor, a brushless dc motor, or a permanent-magnet synchronous motor.

The ADvanced Pow_IR_train board integrates the following features:

- *An integrated power module* from International Rectifier. The ADvanced Pow_IR_train board includes a power module that is capable of driving a 1-hp, three-phase motor. The module integrates a three-phase diode bridge that may be used to rectify a 50/60 Hz three-phase supply. The power module also includes a three-phase IGBT-based inverter that may be connected directly to a three-phase motor.

- *Interchangeable processor modules* so that the appropriate DSP-based motor controller may be used for your application.

- *A UART interface* to the Windows-based program development environment, the Motion Control Debugger

- *All required gate drive circuitry.* The board takes the PWM signals generated by the processor module and feeds them directly to an International Rectifier IR2132 gate drive circuit that provides the appropriate drive signals for the three low-side and the three-high side switches in the inverter.

- *Protection circuits.* The ADvanced Pow_IR_train provides automatic shutdown of the power stage in the event of an overvoltage, overcurrent, overtemperature, or earth fault condition. The fault signal, passed to the DSP-based controller, may also be used in a suitable interrupt service routine.

- *Sensor circuits.* The ADvanced Pow_IR_train board includes all necessary voltage and current sensing to implement a wide variety of control structures. ▶

*Pow_IR_train is a trademark of International Rectifier Corp.

Selecting Mixed-Signal Components for Digital Communications Systems—Part V

Aliases, images, and spurs

by Dave Robertson

Part I (Analog Dialogue 30-3) provided an introduction to the concept of channel capacity, and its dependence on bandwidth and SNR; part II (30-4) briefly summarized different types of modulation schemes; part III (31-1) discussed different approaches to sharing the communications channel, including some of the problems associated with signal strength variability. Part IV (31-2) examined some of the architectural trade-offs used in digital communications receivers, including the problems with frequency translation and the factors contributing to dynamic range requirements. This final installment considers issues relating to the interface between continuous-time and sampled data, and discusses sources of spurious signals, particularly in the transmit path.

Digital communications systems must usually meet specifications and constraints in both the time domain (e.g., settling time) and the frequency domain (e.g., signal-to-noise ratio). As an added complication, designers of systems that operate across the boundary of continuous time and discrete time (sampled) signals must contend with aliasing and imaging problems. Virtually all digital communications systems fall into this class, and sampled-data constraints can have a significant impact on system performance. In most digital communications systems, the continuous-time-to-discrete-time interface occurs in the digital-to-analog (DAC) and analog-to-digital (ADC) conversion process, which is the interface between the digital and analog domains. The nature of this interface requires clear understanding, since the level-sensitive artifacts associated with conversion between digital and analog domains (e.g., quantization) are often confused with the time-sensitive problems of conversion between discrete time and continuous time (e.g., aliasing). The two phenomena are different, and the subtle distinctions can be important in designing and debugging systems. (Note: all digital signals must inherently be discrete-time, but analog signal processing, though generally continuous-time, may also be in discrete time—for example, with switched-capacitor circuits.)

The Nyquist theorem expresses the fundamental limitation in trying to represent a continuous-time signal with discrete samples. Basically, data with a sample rate of F_s samples per second can effectively represent a signal of bandwidth up to $F_s/2$ Hz. Sampling signals with greater bandwidth produces *aliasing*: signal content at frequencies greater than $F_s/2$ is folded, or aliased, back into the $F_s/2$ band. This can create serious problems: once the data has been sampled, there is no way to determine which signal components are from the desired band and which are aliased.

Most digital communications systems deal with band-limited signals, either because of fundamental channel bandwidths (as in an ADSL twisted-pair modem) or regulatory constraints (as with radio broadcasting and cellular telephony). In many cases, the signal bandwidth is very carefully defined as part of the standard for the application; for example, the GSM standard for cellular telephony defines a signal bandwidth of about 200 kHz, IS-95 cellular telephony uses a bandwidth of 1.25 MHz, and a DMT-ADSL twisted-pair modem utilizes a bandwidth of 1.1 MHz . In each case, the Nyquist criterion can be used to establish the *minimum* acceptable data rate to unambiguously represent these signals: 400 kHz, 2.5 MHz, and 2.2 MHz, respectively. Filtering must be used carefully to eliminate signal content outside of this desired bandwidth. The analog filter preceding an ADC is usually referred to as an *anti-alias filter*, since its function is to attenuate signals beyond the Nyquist bandwidth prior to the sampling action of the A/D converter. An equivalent filtering function follows a D/A converter, often referred to as a *smoothing filter*, or *reconstruction filter*. This continuous-time analog filter attenuates the unwanted frequency images that occur at the output of the D/A converter.

At first glance, the requirements of an anti-alias filter are fairly straightforward: the passband must of course accurately pass the desired input signals. The stopband must attenuate any interferer outside the passband sufficiently that its residue (remnant *after* the filter) will not hurt the system performance when aliased into the passband after sampling by the A/D converter. Actual design of anti-alias filters can be very challenging. If out-of-band interferers are both very strong and very near the pass frequency of the desired signal, the requirements for filter stopband and narrowness of the transition band can be quite severe. Severe filter requirements call for high-order filters using topologies that feature aggressive filter roll-off. Unfortunately, topologies of filters having such characteristics (e.g., Chebychev) typically place costly requirements on component match and tend to introduce phase distortion at the edge of the passband, jeopardizing signal recovery.

Designers must also be aware of distortion requirements for anti-alias filters: in general, the pass-band distortion of the analog anti-alias filters should be at least as good as the A/D converter (since any out-of-band harmonics introduced will be aliased). Even if strong interferers are not present, *noise* must be considered in anti-alias filter design. Out-of-band noise is aliased back into the baseband, just like out-of-band interferers. For example, if the filter preceding the converter has a bandwidth of twice the Nyquist band, signal-to-noise (SNR) will be degraded by 3 dB (assuming white noise), while a bandwidth of 4× Nyquist would introduce a degradation of 6 dB. Of course, if SNR is more than adequate, wide-band noise may not be a dominant constraint.

Aliasing has a frequency translation aspect, which can be exploited to advantage through the technique of *undersampling*. To understand undersampling, one must consider the definition of the Nyquist constraint carefully. Note that sampling a signal of *bandwidth, $F_s/2$*, requires a minimum sample rate $\geq F_s$. This $F_s/2$ bandwidth can theoretically be located anywhere in the frequency spectrum [e.g., NF_s to $(N+1/2)F_s$], not simply from dc to $F_s/2$. The aliasing action, like a mixer, can be used to translate an RF or IF frequency down to the baseband. Essentially, signals in the bands $NF_s<\text{signal}<(N+1/2)F_s$ will be translated down intact, signals in the bands $(N–1/2)F_s<\text{signal}<NF_s$ will be translated "flipped" in frequency (see Figure 1) This "flipping" action is identical to the effect seen in high-side injection mixing, and needs to be considered carefully if aliasing is to be used as part of the signal processing. The anti-alias filter in a conventional baseband system is a low-pass filter. In undersampling systems, the anti-alias filter must be a bandpass function.

Undersampling offers several more challenges for the A/D converter designer: the higher speed input signals not only require wider input bandwidth on the A/D converter's sample-and-hold (SHA) circuit; they also impose tighter requirements on the jitter performance of the A/D converter and its sampling clock. To illustrate, compare a baseband system sampling a 100-kHz sine-wave signal and an IF undersampling system sampling a 100-MHz sine-wave signal. In the baseband system, a jitter error of 100 ps produces a maximum signal error of 0.003% of full scale (peak-to-peak)—probably of no concern. In the IF undersampling case, the same 100-ps error produces a maximum signal error of 3% of full scale.
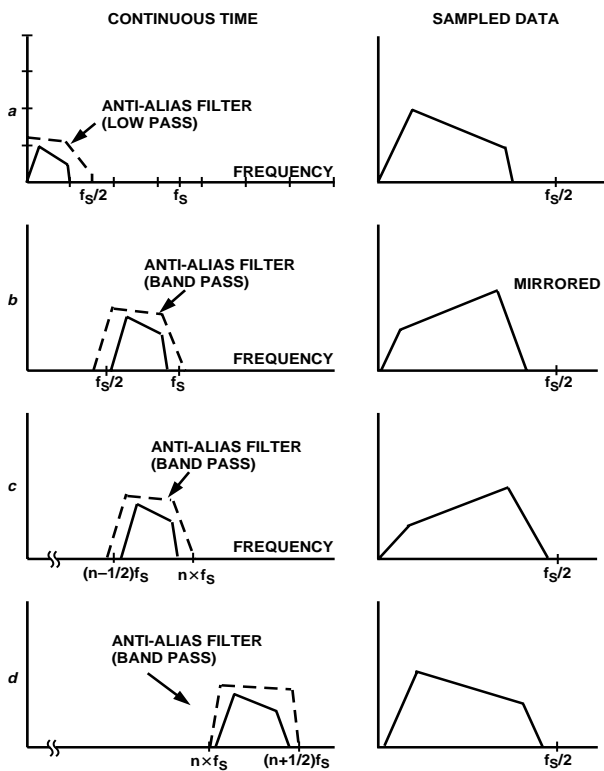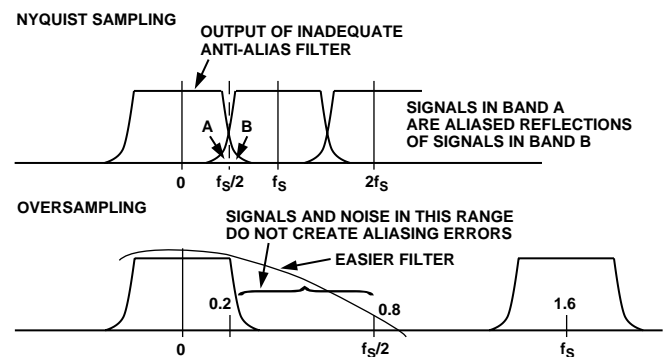

Figure 2. Oversampling makes filtering easier.

Of course, if interferers at frequencies close to 200 kHz are very strong compared to the desired signal, additional dynamic range will be required in the converter to allow it to capture both signals without clipping (see part IV, *Analog Dialogue* 31-2, for a discussion of dynamic range issues.) After conversion, oversampled data may be passed directly to a digital demodulator, or *decimated* to a data rate closer to Nyquist. Decimation involves reducing the digital sampling rate through a digital filtering operation analogous to the analog anti-aliasing filter. A well-designed digital decimation filter provides the additional advantage of reducing the quantization noise from the A/D conversion. For a conventional A/D converter, a *conversion gain* correspnding to a 3-dB reduction in quantization noise is realized for every octave (factor-of-two) decimation. Using the 1.6-MHz sample rate for oversampling as above, and decimating down to the Nyquist rate of 400 kHz, we can realize up to 6 dB in SNR gain (two octaves).

Noise-shaping converters, such as sigma-delta modulators, are a special case of oversampling converters. The sampling rate of the modulator is its high-speed clock rate, and the antialiasing filter can be quite simple. Sigma delta modulators use feedback circuitry to shape the frequency content of quantization noise, pushing it to frequencies away from the signal band of interest, where it can be filtered away. This is possible only in an oversampled system, since by definition oversampled systems provide frequency space beyond the signal band of interest. Where conventional converters allow for a 3-dB/octave conversion gain through decimation, sigma-delta converters can provide 9-, 15-, 21- or more dB/octave gain, depending on the nature of the modulator design (high-order loops, or cascade architectures, provide more-aggressive performance gains).

In a conventional converter, quantization noise is often approximated as "white"—spread evenly across the frequency spectrum. For an N-bit converter, the full-scale signal-to-quantization noise ratio (SQNR) will be $(6.02 N + 1.76)$ dB over the bandwidth from 0 to $F_s/2$. The "white" noise approximation works reasonably well for most cases, but trouble can arise when the clock and single-tone analog frequency are related through simple integer ratios—for example, when the analog input is exactly 1/4 the clock rate. In such cases, the quantization noise tends to "clump" into spurs, a considerable departure from white noise.

Figure 1. Aliasing, and frequency translation through undersampling.

Oversampling is not quite the opposite of undersampling (in fact, it is possible to have a system that is simultaneously oversampling and undersampling). Oversampling involves sampling the desired signal at a rate greater than that suggested by the Nyquist criterion: for example, sampling a 200-kHz signal at 1.6 MHz, rather than the minimum 400 kHz required. The oversampling ratio is defined:

$$OSR = sample\ rate/(2 \times input\ bandwidth)$$

Oversampling offers several attractive advantages (Figure 2). The higher sampling rate may significantly ease the transition band requirements of the anti-alias filter. In the example above, sampling a 200-kHz bandwidth signal at 400 kHz requires a "perfect" brick-wall anti-alias filter, since interferers at 201 kHz will alias in-band to 199 kHz. (Since "perfect" filters are impossible, most systems employ some degree of oversampling, or rely on system specifications to provide frequency guard-bands, which rule out interferers at immediately adjacent frequencies). On the other hand, sampling at 1.6 MHz moves the first critical alias frequency out to 1.4 MHz, allowing up to 1.2 MHz of transition band for the anti-alias filter.

While much has been written in recent years about anti-aliasing and undersampling operations for A/D converters, corresponding filter problems at the output of D/A converters have enjoyed far less visibility. In the case of a D/A converter, it is not unpredictable interferers that are a concern, but the very predictable frequency images of the DAC output signal. For a better understanding of the DAC image phenomenon, Figure 3(a,b) illustrates an ideal

sine wave and DAC output in both the time and frequency domains. It is important to realize that these frequency images are *not* the result of amplitude quantization: they exist even with a "perfect" high-resolution DAC. The cause of the images is the fact that the D/A converter output exactly matches the desired signal only *once* during each clock cycle. During the rest of the clock cycle, the DAC output and ideal signal differ, creating error energy. The corresponding frequency plot for this time-domain error appears as a set of Fourier-series image frequencies (c). For an output signal at frequency F_{out} synthesized with a DAC updated at F_{clock}, images appear at $NF_{clock} \pm F_{out}$. The amplitude of these images rolls off with increasing frequency according to

$$\frac{\sin \pi (F_{out}/F_{clock})}{\pi (F_{out}/F_{clock})}$$

leaving "nulls" of very weak image energy around the integer multiples of the clock frequency. Most DAC outputs will feature some degree of clock feedthrough, which may exhibit itself as spectral energy at multiples of the clock. This produces a frequency spectrum like the one shown in Figure 4.
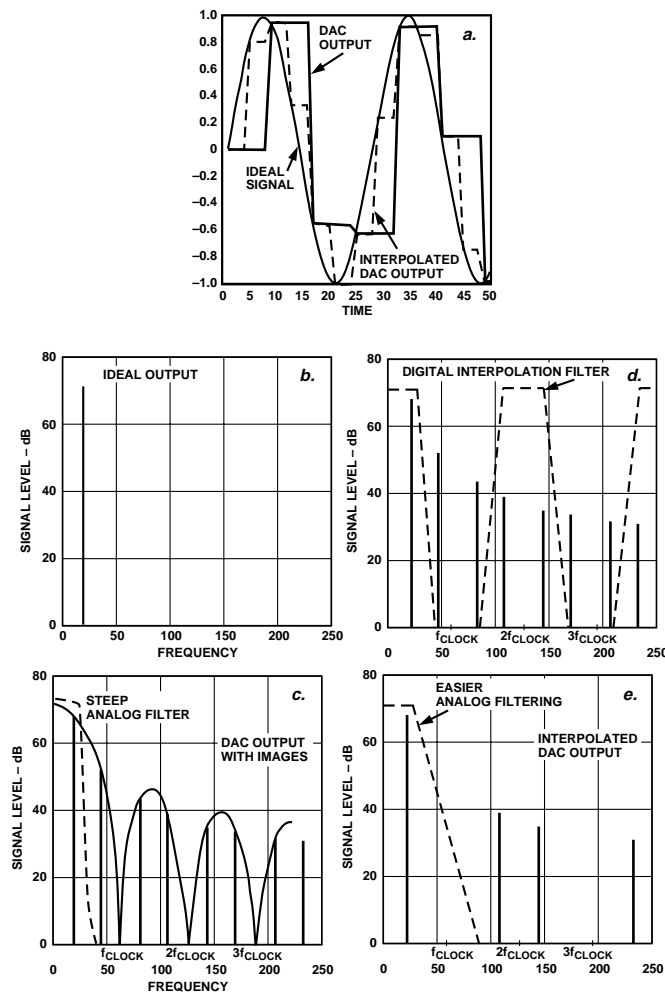

Figure 3. Time domain and frequency domain representation of continuous time and discrete sampled sine wave, and an interpolated discrete sampled sine wave.

The task of the DAC reconstruction filter is to pass the highest desired output frequency, F_{outmax}, and block the lowest image frequency, located at $F_{clock} - F_{outmax}$, implying a smoothing filter transition band of $F_{clock} - 2F_{outmax}$.

This suggests that as one tries to synthesize signals close to the Nyquist limit ($F_{outmax} = F_{clock}/2$), the filter transition gets impossibly steep. To keep the filter problem tractable, many designers use the rule of thumb that the DAC clock should be at least three times the maximum desired output frequency. In addition to the filter difficulties, higher frequency outputs may become noticeably attenuated by the sinx/x envelope: a signal at $F_{clock}/3$ is attenuated by 1.65 dB, a signal at $F_{clock}/2$ is attenuated by 3.92 dB.

Oversampling can ameliorate the D/A filter problem, just as it helps in the ADC case. (More so, in fact, since one need not worry about the strong-interferer problem.) The D/A requires an *interpolation filter*. A digital interpolation filter increases the effective data rate of the D/A by generating intermediate digital samples of the desired signal, as shown in Figure 3(a). The frequency-domain results are shown in (d,e): in this case 2× interpolation has suppressed the DAC output's first two images, increasing the available transition bandwidth for the reconstruction filter from $F_{clock} - 2F_{outmax}$ to $2F_{clock} - 2F_{outmax}$. This allows simplification of the filter and may allow more-conservative pole placement—to reduce the passband phase distortion problems that are the frequent side effects of analog filters. Digital interpolation filters may be implemented with programmable DSP, with ASICs, even by integration with the D/A converter (e.g., AD9761, AD9774). Just as with analog filters, critical performance considerations for the interpolation filters are passband flatness, stop-band rejection (how much are the images suppressed?) and narrowness of the transition band (how much of the theoretical Nyquist bandwidth ($F_{clock}/2$) is allowed in the passband?)

DACs can be used in undersampling applications, but with less efficacy than are ADCs. Instead of using a low-pass reconstruction filter to *reject* unwanted images, a bandpass reconstruction filter can be used to *select* one of the images (instead of the fundamental). This is analogous to the ADC undersampling, but with a few complications. As Figure 3 shows, the image amplitudes are actually points on a sinx/x envelope in the frequency domain. The decreasing amplitude of sinx/x with frequency suggests that the higher frequency images will be attenuated, and the amount of attenuation may vary greatly depending on where the output frequency is located with respect to multiples of the clock frequency. The sinx/x envelope is the result of the DAC's "zero-order-hold" effect (the DAC output remains fixed at target output for most of clock cycle). This is advantageous for baseband DACs, but for an undersampling application, a "return-to-zero" DAC that outputs ideal impulses would not suffer from attenuation at the higher frequencies. Since ideal impulses are physically impractical, actual return-to-zero DACs will have some rolloff of their frequency-domain envelopes. This effect can be pre-compensated with digital filtering, but degradation of DAC dynamic performance at higher output frequencies generally limits the attractiveness of DAC undersampling approaches.

Frequency-domain images are but one of the many sources of spurious energy in a DAC output spectrum. While the images discussed above exist even when the D/A converter is itself "perfect", most of the other sources of spurious energy are the result of D/A converter non-idealities. In communications applications, the transmitter signal processing must ensure that these spurious outputs fall below specified levels to ensure that they do not create interference with other signals in the communications medium. Several specifications can be used

to measure the dynamic performance of D/A converters in the frequency domain (see Figure 4):

- *Spurious-free dynamic range* (SFDR)—the difference in signal strength (dB) between the desired signal (could be single tone or multi-tone) and the highest spurious signal in the band being measured (Figure 4). Often, the strongest spurious response is one of the harmonics of the desired output signal. In some applications, the SFDR may be specified over a very narrow range that does not include any harmonics. For narrowband transmitters, where the DAC is processing a signal that looks similar to a single strong tone, SFDR is often the primary spec of interest.

- *Total harmonic distortion* (THD)—while SFDR indicates the strength of the highest single spur in a measured band, THD adds the energy of all the harmonic spurs (say, the first 8).

- *Two-tone intermodulation distortion* (IMD)—if the D/A converter has nonlinearities, it will produce a mixing action between synthesized signals. For example, if a nonlinear DAC tries to synthesize signals at 1.1 and 1.2 MHz, second-order intermodulation products will be generated at 100 kHz (difference frequency) and 2.3 MHz (sum frequency). Third-order intermodulation products will be generated at 1.3 MHz ($2 \times 1.2 - 1.1$) and 1.0 MHz ($2 \times 1.1 - 1.2$). The application determines which intermodulation products present the greatest problems, but the third-order products are generally more troublesome, because their frequencies tend to be very close to those of the original signals.

- *Signal-to-noise-plus-distortion* (SINAD)—THD measures just the unwanted harmonic energy. SINAD measures all the non-signal based energy in the specified portion of the spectrum, including thermal noise, quantization noise, harmonic spurs, and non-harmonically related spurious signals. CDMA (code-division, multiple-access) systems, for example, are concerned with the total noise energy in a specified bandwidth: SINAD is a more-accurate figure of merit for these applications. SINAD is probably the most difficult measurement to make, since many spectrum analyzers don't have low-enough input noise. The most straightforward way to measure a DAC's SINAD is with an ADC of significantly superior performance.

These specifications, or others derived from them, represent the primary measures of a DAC's performance in signal-synthesis applications. Besides these, there are a number of conventional DAC specifications, many associated with video DACs or other applications, that are still prevalent on DAC data sheets. These include integral nonlinearity (INL), differential nonlinearity (DNL), glitch energy (more accurately, glitch *impulse*), settling time, differential gain and differential phase. While there may be some correlation between these time-domain specifications and the true dynamic measures, the time-domain specs aren't as good at predicting dynamic performance.

Even when looking at dynamic characteristics, such as SFDR and SINAD, it is very important to keep in mind the specific nature of the signal to be synthesized. Simple modulation approaches like QPSK tend to produce strong narrowband signals. The DAC's SFDR performance recreating a single tone near full scale will probably be a good indicator of the part's suitability for the application. On the other hand, modern systems often feature signals with much different characteristics, such as simultaneously synthesized multiple tones (for wideband radios or discrete-multi-tone (DMT) modulation schemes) and direct sequence spread-spectrum modulations (such as CDMA). These more-complicated signals, which tend to spend much more time in the vicinity of the DAC's mid- and lower-scale transitions, are sensitive to different aspects of D/A converter performance than systems synthesizing strong single-tone sine waves. Since simulation models are not yet sophisticated enough to properly capture the subtleties of these differences, the safest approach is to characterize the DAC under conditions that closely mimic the end application. Such requirements for characterization over a large variety of conditions accounts for the growth in the size and richness of the datasheets for D/A converters. ▶

For Further Reading:

For detailed discussion of discrete time artifacts and the Nyquist Theorem: Oppenheim, Alan V. and Schaeffer, Ronald W, *Discrete-Time Signal Processing*. Englewood Cliffs, NJ: Prentice Hall, 1989.

For more details on sigma-delta signal processing and noise shaping: Norsworthy, Steven R, Schreier; Richard; Temes, Gabor C., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press, 1997.

For more details on DAC spectral phenomena: Hendriks, Paul, "Specifying Communication DACs", *IEEE Spectrum* magazine, July, 1997, pages 58-69.
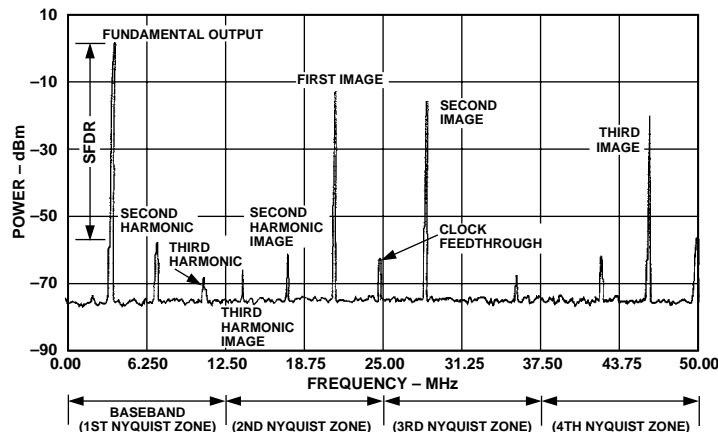

Figure 4. Different error effects in the output spectrum of a DAC.

DSP 101 Part 3: Implement Algorithms on a Hardware Platform

by Noam Levine and David Skolnick

So far, we have described the physical architecture of the DSP processor, explained how DSP can provide some advantages over traditionally analog circuitry, and examined digital filtering, showing how the programmable nature of DSP lends itself to such algorithms. Now we look at the process of implementing a finite-impulse-response (FIR) filter algorithm (briefly introduced in Part 2, implemented in ADSP-2100 Family assembly code) on a hardware platform, the ADSP-2181 EZ-Kit Lite™. The implementation is expanded to handle data I/O issues.

USING DIGITAL FILTERS

Many of the architectural features of the DSP, such as the ability to perform zero-overhead loops, and to fetch two data values in a single processor cycle, will be useful in implementing this filter.

Reviewing briefly, an FIR filter is an all-zeros filter that is calculated by convolving an input data-point series with filter coefficients. Its governing equation and direct-form representation are shown in Figure 1.
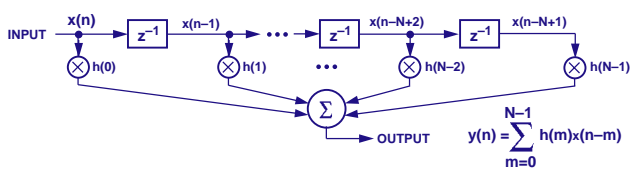

Figure 1. Direct-form FIR filter structure.

In this structure, each "z^{-1}" box represents a single increment of history of the input data in z-transform notation. Each of the successively delayed samples is multiplied by the appropriate coefficient value, $h(m)$, and the results, added together, generate a single value representing the output corresponding to the nth input sample. The number of delay elements, or filter taps, and their coefficient values, determine the filter's performance.

The filter structure suggests the physical elements needed to implement this algorithm by computation using a DSP. For the computation itself, each output sample requires a number of multiply-accumulate operations equal to the length of the filter.

The delay line for input data and the coefficient value list require reserved areas of memory in the DSP for storing data values and coefficients. The DSP's enhanced Harvard architecture lets programmers store data in Program Memory as well as in Data Memory, and thus perform two simultaneous memory accesses in every cycle from the DSP's internal SRAM. With Data Memory holding the incoming samples, and Program Memory storing the coefficient values, both a data value and a coefficient value can be fetched in a single cycle for computation.

This DSP architecture favors programs that use circular buffering (discussed briefly in Part 2 and later in this installment). The implication is that address pointers need to be initialized only at the beginning of the program, and the circular buffering mechanism ensures that the pointer does not leave the bounds of its assigned memory buffer—a capability used extensively in the FIR filter code for both input delay line and coefficients. Once the elements of the program have been determined, the next step is to develop the DSP source code to implement the algorithm.

DEVELOPING DSP SOFTWARE

Software development flow for the ADSP-2100 Family consists of the following steps: architecture description, source-code generation, software validation (debugging), and hardware implementation. Figure 2 shows a typical development cycle.
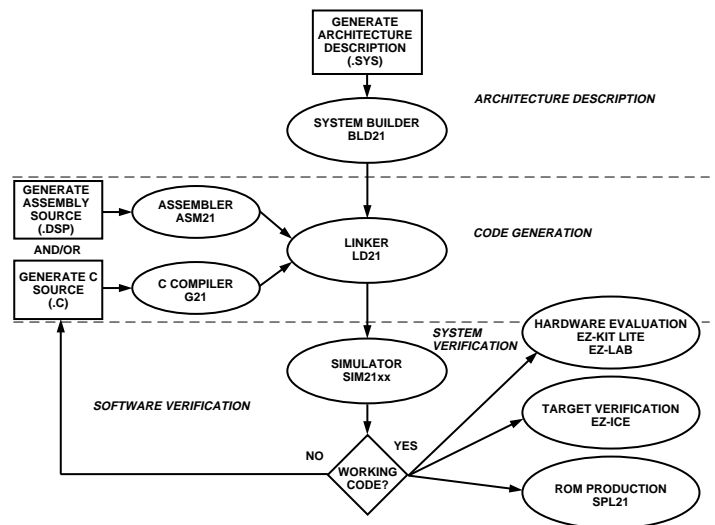
Figure 2. Software development flow.

Architecture description: First, the user creates a software description of the hardware system on which the algorithm runs. The system description file includes all available memory in the system and any memory-mapped external peripherals. Below is an example of this process using the ADSP-2181 EZ-Kit Lite.

Source-code generation: Moving from theory into practice, this step—where an algorithmic idea is turned into code that runs on the DSP—is often the most time-consuming step in the process. There are several ways to generate source code. Some programmers prefer to code their algorithms in a high-level language such as C; others prefer to use the processor's native assembly language. Implementations in C may be faster for the programmer to develop, but compiled DSP code lacks efficiency by not taking full advantage of a processor's architecture.

Assembly code, by taking full advantage of a processor's design, yields highly efficient implementations. But the programmer needs to become familiar with the processor's native assembly language. Most effective is combining C for high-level program-control functions and assembly code for the time-critical, math-intensive portions of the system. In any case, the programmer must be aware of the processor's system constraints and peripheral specifics. The FIR filter system example in this article uses the native assembly language of the ADSP-2100 Family.

Software validation ("debugging"): This phase tests the results of code generation—using a software tool known as a *simulator*—to check the logical flow of the program and verify that an algorithm is performing as intended. The simulator is a model of the DSP processor that a) provides visibility into all memory locations and processor registers, b) allows the user to run the DSP code either

continuously or one instruction at a time, and c) can simulate external devices feeding data to the processor.

Hardware implementation: Here the code is run on a real DSP, typically in several phases: a) tryout on an evaluation platform such as EZ-Kit Lite; b) in-circuit emulation, and c) production ROM generation. *Tryout* provides a quick go/no-go determination of the program's operation; this technique is the implementation method used in this article. *In-circuit emulation* monitors software debug in the system, where a tool such as an EZ-ICE™ controls processor operation on the target platform. After all debug is complete, a *boot ROM* of the final code can be generated; it serves as the final production implementation.

WORKING WITH THE ADSP-2181 EZ-KIT LITE

Our example of the development cycle walks through the process, using the ADSP-2181 EZ-Kit Lite (development package ADDS-21xx-EZLITE) as the target hardware for the filter algorithm. The EZ-Kit Lite, a low-cost demonstration and development platform, consists of a 33-MHz ADSP-2181 processor, an AD1847 stereo audio codec, and a socketed EPROM, which contains monitor code for downloading new algorithms to the DSP through an RS-232 connection (Figure 3).
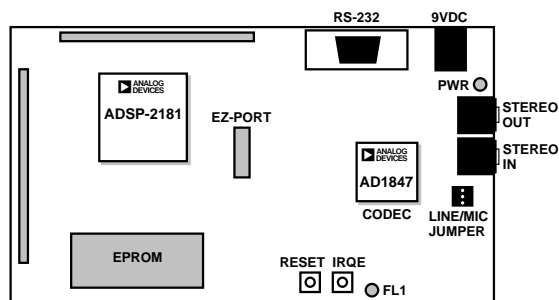

Figure 3. Layout of EZ-Kit Lite board.

To complete the architecture description phase, one needs to know the memory and memory-mapped peripherals that the DSP has available to it. Programmers store this information in a system-description file so that the development tools software can produce appropriate code for the target system. The EZ-Kit Lite needs no memory external to the DSP, because available memory on-chip consists of the 16,384 locations of the ADSP-2181's Program Memory (PM) SRAM, and 16,352 locations of Data Memory (DM) SRAM. (32 DM locations used for system control registers are not available for working code). More information on the ADSP-2181, the EZ-Kit Lite's architecture, and related topics, can be found in texts mentioned at the end of this article.

Available system resources information is recorded in a system description file for use by the ADSP-2100 Family development tools. A system description file has a .SYS extension. The following list shows a system description file [EZKIT_LT.SYS]:

```
.system   EZ_LITE;        /* gives a name to this system */
.adsp2181;                /* specifies the processor      */
.mmap0;                   /* specifies that the system boots and that */,
                          /* PM location 0 is in internal memory    */
.seg/PM/RAM/ABS=0/code/data       int_pm[16384];
.seg/DM/RAM/ABS=0                 int_dm[16352];
.endsys;                  /* ends the description */
```

The listing declares 16,384 locations of PM as RAM, starting at address 0, to let both code segments and data values be placed there. Also declared are 16,352 available locations of data memory as RAM, starting at address 0. Because these processors use a Harvard architecture with two distinct memory spaces, PM address 0 is distinct from DM address 0. The ADSP-2181 EZ-Kit Lite's codec is connected to the DSP using a serial port, which is not declared in the system description file. To make the system description file available to other software tools, the System Builder utility, BLD21, converts the .SYS file into an architecture, or .ACH, file. The output of the System Builder is a file named EZKIT_LT.ACH.

After writing the code (page 15), the next step is to generate an executable file, i.e., turn the code into instructions that the DSP can execute. First one *assembles* the DSP code. This converts the program file into a format that the other development tools can process. Assembling also checks the code for syntax errors. Next, one *links* the code to generate the DSP executable, using the available memory that is declared in the architecture file. The Linker fits all of the code and data from the source code into the memory space; the output is a DSP executable file, which can be downloaded to the EZ-Kit Lite board.

GENERATING FILTER CODE

Part 2 of this series [Analog Dialogue 31-2, page 14, Figure 6] introduced a small assembly code listing for an FIR filter. Here, that code is augmented to incorporate some EZ-Kit Lite-specific features, specifically codec initialization and data I/O. The core filter-algorithm elements (multiply-accumulates, data addressing using circular buffers for both data and coefficients, and reliance on the efficiency of the zero-overhead loop) do not change.

The incoming data will be sampled using the on-board AD1847 codec, which has programmable sampling rate, input gain, output attenuation, input selection, and input mixing. Its programmable nature makes the system flexible, but it also adds a task of programming to initialize it for the DSP system.

ACCESSING DATA

For this example, a series of control words to the codec—to be defined at the beginning of the program in the first section of the listing—will initialize it for an 8-kHz sampling rate, with moderate gain values on each of the input channels. Since the AD1847 is programmable, users would typically reuse interface and initialization code segments, changing only the specific register values for different applications. This example will add the specific filter segment to an existing code segment found in the EZ-Kit Lite software.

This interface code declares two areas in memory to be used for data I/O: "tx_buf", for data to be transmitted out of the codec, and "rx_buf", where incoming data is received. Each of these memory areas, or buffers, contains three elements, a control or status word, left-channel data, and right-channel data. For each sample period, the DSP will *receive* from the codec a status word, left channel data, and right channel data. On every sample period, the DSP must supply to the codec a *transmit* control word, left channel data, and right channel data. In this application, the control information sent to the codec will not be altered, so the first word in the transmit data buffer will be left as is. We will assume that the source is a monophonic microphone, using the right channel (no concern about left-channel input data).

Using the I/O shell program found in the EZ-Kit Lite software, we need only be involved with the section of code labeled "input_samples". This section of code is accessed when new data is received from the codec ready to be processed. If only the right channel data is required, we need to read the data located in data memory at location rx_buf + 2, and place it in a data register to be fed into the filter program.

The data arriving from the codec needs to be fed into the filter algorithm via the input delay line, using the circular buffering capability of the ADSP-2181. The length of the input delay line is determined by the number of coefficients used for the filter. Because the data buffer is circular, the oldest data value in the buffer will be wherever the pointer is pointing after the last filter access (Figure 4) . Likewise the coefficients, always accessed in the same order every time through the filter, are placed in a circular buffer in Program Memory.
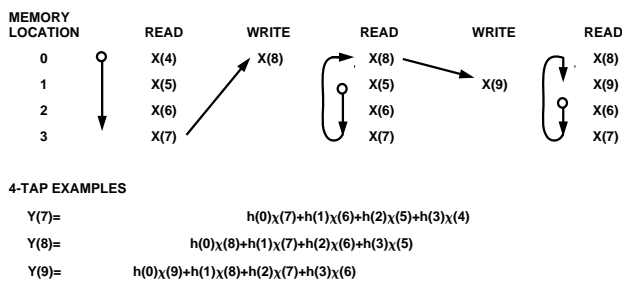

4-TAP EXAMPLES

$Y(7) = h(0)\chi(7) + h(1)\chi(6) + h(2)\chi(5) + h(3)\chi(4)$

$Y(8) = h(0)\chi(8) + h(1)\chi(7) + h(2)\chi(6) + h(3)\chi(5)$

$Y(9) = h(0)\chi(9) + h(1)\chi(8) + h(2)\chi(7) + h(3)\chi(6)$

Figure 4. Example of using circular buffers for filter data input.

Algorithm Code

To operate on the received data, the code section published in the last installment can be used with few modifications. To implement this filter, we need to use the multiply/accumulate (MAC) computational unit and the data address-generators.

The ADSP-2181's MAC stores the result in a 40-bit register (32 bits for the product of 2 16-bit words, and 8 bits to allow the sum to expand without overflowing). This allows intermediate filter values to grow and shrink as necessary without corrupting data. The code segment being used is generic (i.e., can be used for any length filters); so the MAC's extra output bits allow arbitrary filters with unknown data to be run with little fear of losing data.

To implement the FIR filter, the multiply/accumulate operation is repeated for all taps of the filter on each data point. To do this (and be ready for the next data point), the MAC instruction is written in the form of a loop. The ADSP-21xx's zero-overhead loop capability allows the MAC instruction to be repeated for a specified number of counts without programming intervention. A counter is set to the number of taps minus one, and the loop mechanism automatically decrements the counter for each loop operation. Setting the loop counter to "taps–1" ensures that the data pointers end up in the correct location after execution is finished and allows the final MAC operation to include rounding. As the AD1847 is a 16-bit codec, the MAC with rounding provides a statistically unbiased result rounded to the nearest 16-bit value. This final result is written to the codec.

For optimal code execution, every instruction cycle should perform a meaningful mathematical calculation. The ADSP-21xxs accomplish this with multi-function instructions: the processor can perform several functions in the same instruction cycle. For the FIR filter code, each multiply-accumulate (MAC) operation

can be performed in parallel with two data accesses, one from Data Memory, one from Program Memory. This capability means that on every loop iteration a MAC operation is being performed. At the same time, the next data value and coefficient are being fetched, and the counter is automatically decremented. All without wasting time maintaining loops.

As the filter code is executed for each input data sample, the output of the MAC loop will be written to the output data buffer, tx_buf. Although this program only deals with single-channel input data, the result will be written out to both channels by writing to memory buffer addresses tx_buf+1 and tx_buf+2.

The final source code listing is shown on page 15. The filter algorithm itself is listed under "Interrupt service routines". The rest of the code is used for codec and DSP initialization and interrupt service routine definition. Those topics will be explored in future installments of this series.

THE EZ-KIT LITE
The Windows-based monitor software provided with the EZ-Kit Lite, makes it possible to load an executable file into the ADSP-2181 on the EZ-Kit Lite board. This is accomplished through the pull-down "Loading" menu by selecting "Download user program and Go" (Figure 5). This will download the filter program to the ADSP-2181 and start program execution.
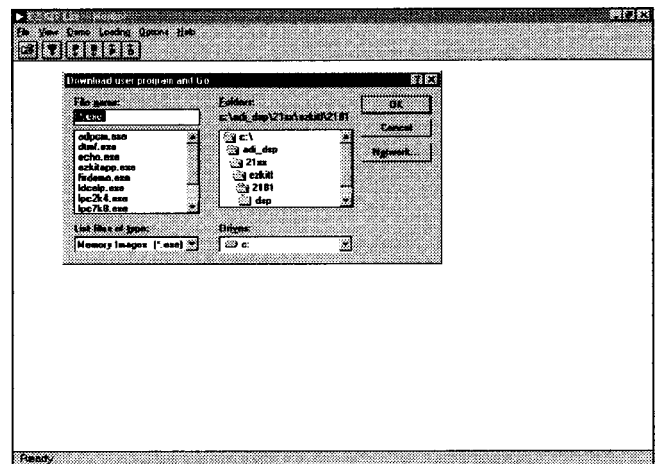
Figure 5. EZ-Kit Lite download menu.

REVIEW AND PREVIEW
The goal of this article was to outline the steps from an algorithm description to a DSP executable program that could be run on a hardware development platform. Issues introduced include software development flow, architecture description, source-code generation, data I/O, and the EZ-Kit Lite hardware platform

There are many levels of detail associated with each of these topics that this brief article could not do justice to. Further information is available in the references below. The series will continue to build on this application with additional topics. The next article will examine data input/output (I/O) issues in greater detail through the processor interrupt structure, and discuss additional features of the simple filter algorithm.

REFERENCES
ADSP-2100 Family Assembler Tools & Simulator Manual. Consult your local Analog Devices Sales Office.

ADSP-2100 Family User's Manual. Analog Devices. Free. **Circle 4** ▶

FIR Filter code listing for EZ-Kit Lite

```
/************************************************************
*
* hello81.dsp — template file for 2181 ez-kit lite board
*
* This sample program is organized into the following sections:
*
* Assemble time constants (system.h)
* Interrupt vector table
* ADSP 2181 intialization (init1847.dsp)
* ADSP 1847 codec intialization (init1847.dsp)
* Interrupt service routines
*
* This program implements a simple 'talk-through' with the AD1847 codec.
* The initialization routines have been put into the init1847.dsp file. This
* file contains the interrupt vector table, the main 'dummy' loop, and the
* interrupt service routines for the pushbutton and the serial port 0 receive.
* The pushbutton (IRQE) causes the LED on the EZ-Kit board to toggle
* with  each button press.
*
* Parameters controlling the sampling rate, gains, etc., are contained in the
* file init1847.dsp. Serial Port 0 is used to communicate with the AD1847.
* The transmit interrupts are used to configure the codec, then they are
* disabled and the receive interrupts are used to implement the 'talk-through'
* audio.
*
* The definitions for the memory-mapped control registers are contained in
* the file: system.h
*
* The application can be built by:
*
* asm21 -c -l -2181 hello81
* asm21 -c -l -2181 init1847
* ld21 hello81 init1847 -a 2181 -e hello81 -g -x
*
************************************************************/
.module/RAM/ABS=0 EzHello;
#include <system.h>
#define taps 255                    /* filter tap length */
.var/dm/circ        filt_data[taps];        /* input data buffer */
.var/pm/circ        filt_coeffs[taps];      /* coefficient buffer */
.init filt_coeffs:<coefs.dat>;              /* initialize coefficients */
.external rx_buf, tx_buf;
.external init_cmds, stat_flag;
.external next_cmd, init_1847, init_system_regs, init_sport0;
/************************************************************
* Interrupt vector table
************************************************************/
jump start; rti; rti; rti;          /* 00: reset  */
rti;  rti; rti; rti;                /* 04: IRQ2  */
rti;  rti; rti; rti;                /* 08: IRQL1  */
rti;  rti; rti; rti;                /* 0c: IRQL0  */
ar = dm(stat_flag);                 /* 10: SPORT0 tx */
ar = pass ar;
if eq rti;
jump next_cmd;
jump input_samples;                 /* 14: SPORT1 rx */
   rti; rti; rti;
jump irqe; rti; rti; rti;           /* 18: IRQE  */
rti;   rti; rti; rti;               /* 1c: BDMA  */
rti;   rti; rti; rti;               /* 20: SPORT1 tx or IRQ1 */
rti;   rti; rti; rti;               /* 24: SPORT1 rx or IRQ0 */
rti;   rti; rti; rti;               /* 28: timer  */
rti;   rti; rti; rti;               /* 2c: power down */
/************************************************************
* ADSP 2181 intialization
************************************************************/
```

```
start:
i0 = ^rx_buf;           /* remember codec autobuffering uses i0 and i1 !! */
l0 = %rx_buf;
i1 = ^tx_buf;
l1 = %tx_buf;
i3 = ^init_cmds;        /* i3 can be used for something else after codec init */
l3 = %init_cmds;
m0 = 0;
m1 = 1;
/* initialize serial port 0 for communication with the AD1847 codec */
 call init_sport0;
/* initialize the other system registers, etc. */
 call init_system_regs;
/* initialize the AD1847 codec */
 call init_1847;
 ifc = b#00000011111111;            /* clear any pending interrupt */
 nop;        /* there is a 1 cycle latency for ifc */
/* setup pointers for data and coefficients */
 i2 = ^filt_data;
 l2 = %filt_data;
 i5 = ^filt_coefs;
 m5 = 1;
 l5 = %filt_coefs;
 imask=b#0000110000; /* enable rx0 interrupt */
            /* ||||||||||+ | timer
               |||||||||+- | SPORT1 rec or IRQ0
               ||||||||+-- | SPORT1 trx or IRQ1
               |||||||+--- | BDMA
               ||||||+---- | IRQE
               |||||+----- | SPORT0 rec
               ||||+------ | SPORT0 trx
               |||+------- | IRQL0
               ||+-------- | IRQL1
               |+--------- | IRQ2
 */
/*-----------------------------------------------------------------------
 - wait for interrupt and loop forever
 -----------------------------------------------------------------------*/
talkthru:  idle;
 jump talkthru;
/************************************************************
 * Interrupt service routines
 ************************************************************/
/*-----------------------------------------------------------------------
 - FIR Filter
 -----------------------------------------------------------------------*/
input_samples:
 ena sec_reg;                       /* use shadow register bank */
 ax0 = dm (rx_buf + 1);             /* read data from converter */
 dm(i2,m1) = ax0;                   /* write new data into delay line, pointer
                                    now pointing to oldest data */
 cntr = taps - 1;
 mr = 0, mx0 = dm(i2,m1), my0 = pm(i5,m5); /* clear accumulator, get first
                                    data and coefficient value */
 do filt_loop until ce;            /* set-up zero-overhead loop */
filt_loop: mr = mr + mx0 * my0(ss), mx0 = dm(i2,m1), my0 = pm(i5,m5);
                                    /* MAC and two data fetches */
 mr = mr + mx0 * my0 (rnd); /* final multiply, round to 16-bit result */
 if mv saat mr;                     /* check for overflow */
 dm(tx_buf+1) = mr1;
 dm(tx_buf+2) = mr1;                /* output data to both channels */
 rti;
.endmod;
```

Amplifiers, D/A Converters, References

260-MHz Dual Buffer
AD8079: 0.01% ΔG, 0.02° ΔΦ ±0.1-dB flat to 50 MHz

The AD8079 is a dual fixed gain buffer for video and other wideband applications. It is optionally available with pin-strappable fixed gains of +2, +1, and –1 (A grade) and +2.2, +1, and –1.2 (B grade); the latter permits compensation of system gain losses. The 70-mA output can drive up to 8 video loads. Bandwidth is 260 MHz (–3 dB), and response is flat within ±0.1 dB to >50 MHz.

Typical applications are for differential driving of twisted pair wiring, and for buffering inputs and outputs of switches, such as the AD8116 crosspoint. Differential gain and phase errors are 0.01% and 0.02°, respectively, and crosstalk is –70 dB at 5 MHz. Quiescent dissipation is only 50 mW per amplifier. The device operates on supplies from ±3 V to ±6 V and is available in an 8-pin plastic SOIC. Prices start at $3.50 (1000s).

Faxcode* 2072 or Circle 5 ▶

Triple I_{FB} Op Amp
AD8023 has 250-MHz BW Drives heavy capacitive loads

The AD8023 has a trio of fast-settling current-feedback operational amplifiers with individual Disable on a single silicon chip. They can drive loads (including capacitive) at up to 70 mA, while drawing only 10 mA max quiescent current. This makes the device useful in RGB video systems that require good flatness over a wide bandwidth, while drawing minimal power. Bandwidth is 250 MHz (10 MHz with 0.1-dB flatness), with 1200 V/μs slew rate and 30-ns 0.1% settling (300 pF, 1 kΩ load).

Video differential gain and phase errors are 0.06% and 0.02°. The Disable feature (1.3-mA power-down, high-impedance output) turnoff time is 30 ns. The AD8023 operates (–40 to +85°C) with single (+4.2 to +15 V) or dual (±2.1 to ±7.5 V) supplies, and the device is housed in a 14-lead plastic SOIC. Price (1000s) is $3.99.

Faxcode* 2192 or Circle 6 ▶

μPower References
Low-noise ADR290/291/292 XFET™: Better than bandgap

The ADR290, ADR291, and ADR292 are precision 2.048, 2.5, and 4.096-V low-noise micropower precision references. They employ a new reference technology, XFET™ (eXtra implanted junction FET), offering the benefits of low supply current and very low thermal hysteresis, with substantially lower noise than bandgaps and lower power than buried Zeners.

They are specified for 2.7, 3.0, and 5.0-V min supply voltage, 15, 15, and 18 μA max supply current, 420, 480, and 640 nV/√Hz noise density at 1 kHz. The best grades have initial accuracy to within ±2-mV and 8-ppm /°C tempco. Minimum full-load output current is 5 mA. Each is available in three performance grades specified at –40 to +85°C and –25 to +85°C. They are available in 8-lead SOICs and TO-92s, and 3-pin TSSOPs. Prices start at $1.95 in 1000s.

Faxcode* 2110 or Circle 7 ▶

14-Bit, 125-MSPS D/A
AD9764 TxDAC®: 2.7 to 5.5 V Optimized for SFDR, THD, IMD

The AD9764 brings 14-bit-resolution to the TxDAC® series of high-performance, low-power, pin-compatible CMOS DACs. It is designed for reconstructing wideband, high-dynamic-range signals in communications and test equipment. Its excellent IMD and SFDR performance for single- and multitone signals upgrades existing communication systems and permits new wideband transmit architectures. Its applications include base stations and ADSL & HFC cable modems.

Characteristics include update rate of 100 MSPS min, 125 typical, 2.7 to 5.5-V supply voltage, on-chip reference, 20-mA current output, 45 mW dissipation @ 3V, and Sleep mode. The CMOS device is available in a 28-lead SOIC for temperatures from –40 to +85°C. An evaluation board is available. Prices are $19.18 in 1000s for the AD9764, $150 for the evaluation board.

Faxcode* 2057 or Circle 8 ▶

Dual 10-Bit TxDAC+™
40-MSPS AD9761 for I&Q has dual 2× interpolation filters

The AD9761, the latest addition to ADI's family of transmit DACs, is a subsystem-on-a-chip, based on the TxDAC® core (see adjacent story). It consists of a matched pair of high-performance 40-MSPS 10-bit DACs, optimized for low distortion (58-dB SINAD, 9.5 ENOB, 65-dB SFDR) for flexible handling of QAM I & Q data. Included are a pair of 2× digital interpolation filters with 62.5-dB stop-band rejection and an on-chip 1.2-V reference.

The AD9761 provides 10-mA of output current and operates on a 2.7 to 5.5-V supply with only 200 mW dissipation at 3 V. A Sleep mode reduces input current by a factor of about 9. The DACs share a common 20-MSPS interleaved data interface. Operation is from –40 to +85°C, and the device is housed in a 28-lead SSOP. Its price (1000s) is $11.95.

Faxcode* 2135 or Circle 9 ▶

Dual 8-Bit Serial DAC
Lo-power +2.7/+5.5-V Ad7303 in 8-pin PDIP, SOIC, μSOIC

The AD7303 is a dual 8-bit serial input, voltage-output D/A converter with a supply voltage range of +2.7 to +5.5 V. Its on-chip precision output voltage buffers allow the DAC outputs to swing rail-to-rail. The shared input is a 3-wire serial interface that operates at clock rates up to 30 MHz; it is compatible with QSPI, SPI, microwire, and digital signal-processor interface standards. The control portion of the 16-bit input register addresses the relevant DAC, provides device or chip power-down, selects internal or external reference, and can provide for simultaneous updating.

Ideal for portable battery-operated equipment, the AD7303 consumes only 7.5 mW max at 3 V and less than 3 μW with full power-down. It is available in 8-pin plastic DIP, SOIC, and μSOIC, for –40 to +105°C. Prices start at $2.35 in 1000s.

Faxcode* 2044 or Circle 10 ▶

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Analog-to-Digital Converters

8-Bit, 32-MSPS ADC
Low-$ AD9280: 2.7 to 5.5 V Has 300-MHz analog BW

The AD9280 is a low cost 8-bit, 32-MSPS A/D converter with 2.7 to 5.5-V single-supply operation and low power consumption (95 mW at 3 V). It has a wide-bandwidth input sample-hold (300 MHz), a programmable internal reference, and a flexible input structure. It also incorporates clamping (useful in video "dc restoring"), Sleep mode (to conserve power), an out-of-range indicator, and 3-state output buffers. The AD9280 is used to digitize high-speed analog data in video, CCD signal chains (scanners, etc.), and communications systems.

Performance includes differential non-linearity of 0.2 LSB, and 7.7 ENOB at 16 MHz. The AD9280 is housed in a 28-pin SSOP, for temperatures from –40 to +85°C, and is pin-compatible to the 10-bit AD9200. Price in 1000s is $3.37.

Faxcode* 2163 or Circle 11 ▶

8- & 10-Bit ADCs
2.7 to 5.5-V AD7819/AD7813 have 200/400-ksps thruput

The AD7819 and AD7813 are pin-compatible 8- and 10-bit low-power single-supply sampling A/D converters. They are housed in 16-pin DIP, SOIC and TSSOP packages. Normally dissipating a low 17.5 mW max in full operation, they dissipate 5 μW max in power down; and in the automatic-power-down-between-conversions mode, the AD7813 dissipates only 34.6 μW max at 1 ksps, and 3.5 mW max at 100 ksps.

Both devices have an identical 8-bit parallel interface for easy interfacing to μPs and DSPs. The AD7813 reads out 10 bits with a 2nd 2-bit byte. The AD7819 and AD7813 operate over respective temperature ranges of –40 to +125°C and –40 to +105°C. They can use an external precision reference or the power supply. Prices (1000s) are $1.95 (AD7819) and $2.55 (AD7813).

Faxcode* 2064, 2063 or Circle 12, 13 ▶

4- & 8-Channel ADCs
10-bit serial AD7811/AD7812: 350 ksps thruput, 2.5-5.5 V_S

The AD7811 and AD7812 are 10-bit sampling A/D converters with serial digital interfaces and multiplexed 4- and 8-channel analog inputs. They operate from 2.7 to 5.5-V supplies and have a maximum throughput of 350 ksps. They accept analog inputs over the range of 0 V to +V_{DD}; and users can employ the on-chip references, external precision references, or the supply voltage. Their low power consumption (315 μW at 10 ksps), ability to power down after conversions, and small package size (16-pin TSSOP) make these devices particularly suitable for portable and power-consumption-critical applications.

The serial interface is compatible with the serial interfaces of most μCs and DSPs. A Package Address pin allows bus sharing. Operation is specified from –40 to +105°C. Prices (1000s) are $2.90 and $3.30.

Faxcode* 2062 or Circle 14 ▶

8-, 10-Bit Serial ADCs
AD7823/AD7810 operate on 2.7–5.5 V; 8-pin DIP, SO, μSO

The AD7823 and AD7810 are pin-compatible 8- and 10-bit low-power single-supply sampling A/D converters with serial interfaces and maximum throughput rates of 135 and 350 ksps. They are housed in 8-pin DIP, SOIC and μSOIC packages. Normal dissipation, a low 17.5 mW max in full operation, drops to 5 μW max in power down (data can be read); and in automatic-power-down-between-conversions mode, the AD7810 dissipates only 27 μW max at 1 ksps, and 2.7 mW max at 100 ksps.

Both devices have microcontroller-compatible serial interfaces for fast, easy interfacing. The AD7823 and AD7810 operate over respective temperature ranges of –40 to +125°C and –40 to +105°C. They can use an external precision reference or the power supply. DIP-package prices (1000s) are respectively $1.95 & $2.45.

Faxcode* 2085, 2061 or Circle 15, 16 ▶

24-Bit Σ-Δ ADC
AD7731 has buffered inputs serial interface, on-chip PGA

The AD7731 is a complete 24-bit low-noise (55 nV rms typical), high-throughput A/D converter for industrial measurement and process-control applications. It incorporates a 7-step binary-programmable-gain amplifier, allowing input signal ranges from 20 mV to ±1.28 V. Throughput is programmable, from 50 Hz up to 6400 Hz. The sigma-delta architecture uses an analog modulator and a low-pass programmable digital filter, allowing adjustment of filter cutoff, output rate, and settling time.

Its 3-wire serial output is compatible with microcontrollers & digital signal processors. It operates from a single +5-V power supply and can accept external references ranging from 1 V up to (and including) the +5-V positive rail. It is available for –40 to +85°C packaged in 24-lead PDIP, SO, and TSSOP. 1000-lot price is $9.86.

Faxcode* 2131 or Circle 17 ▶

16-Bit, 5-V ADCs
AD977 upgrades ADS7809 AD977A: 200-ksps thruput

The AD977 and AD977A are 16-bit serial-output A/D converters with a wide choice of analog input ranges (±10 V, ±5 V, ±3.3 V, and 0 to 10, 5, and 4 V). Requiring minimal support circuitry and low power, they contain internal references, provide low cost/performance, and run from a single +5-V supply. Their inputs are protected against voltages up to ±25 V. Consuming only 100 mW, the AD977A runs at 200 ksps (100 ksps for the AD977). In the power-down mode, dissipation is only 50 μW.

The devices contain a successive-approximation ADC, an internal 2.5-V reference, and a high-speed serial interface, and include on-chip clock circuits. Available in 20-lead plastic DIPs and SOICs, and 28-lead SSOPs, they operate from –40 to +85°C. Price (1000s) in PDIP is $20 for AD977, and $26 for AD977A.

Faxcode* 1958 or Circle 18 ▶

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Digital Communication and Supervisory

DECT IF Transceiver
AD6402 integrated subsystem for multichannel base stations

The AD6402 is an IF subsystem used in high-performance TDMA (time-domain multiple access) digital radios employing FSK, GFSK, FM, and QPSK modulation schemes. Designed primarily for digital enhanced cordless communication (DECT), it can be used in any similar radio architecture with 1-MBPS bit rates. Highly integrated, it includes a limiter stage with inter-stage filter, RSSI detection, a PLL demodulator, IF VCO, IF buffers, VCO regulator, and power management.

The AD6402 has multiple power-down modes to maximize battery life. Using an on-chip PLL demodulator, it requires no manufacturing trims; an integrated 2nd IF filter further reduces external component count. It will operate with $\geq$2.7-V supply, is housed in a 28-pin SSOP, and operates from -25 to $+85°C$. Price in 1000s is $6.55.

Faxcode* 2256 or Circle 19 ▶

1-Chip RAS Modem
Interfaces ISP serial T1 or E1 lines to digital network

The ADSP-21mod870 is the world's first complete single-chip digital modem for remote-access servers (RAS). It is optimized for implementing a complete V.34/56K modem. Since its bundled cost includes software, controller, memory, and data pump, it needs no external memory or data controller. At 2.58 cm^2 (0.4 in^2), and dissipating only 140 mW (3.3 V) in the active mode, it has the smallest size and lowest dissipation per channel—plus the lowest cost—among available alternatives.

Based on the ADSP-2100 family architecture, each chip (i.e., modem port) can be reprogrammed on demand. New protocols can be downloaded, existing protocols updated. Any protocols may be loaded automatically depending on the user's modem speed. Packaging is 100-pin TQFP. Bundled per-channel cost is $28.

Circle 20 ▶

MODIO™ HSP Codec
AD1821 single-chip audio & comm subsystem for PCs

The single-chip AD1821 MODIO™ (modem over audio) Soundcomm™ HSP audio and communications subsystem for personal computers includes the AD1821 mixed-signal controller IC and MODIO host signal-processing (HSP) software drivers. It has full legacy compatibility with applications written for Soundblaster Pro and AdLib, also servicing Microsoft PC 97 applications.

Included are an OPL3-compatible music synthesizer, Phat™ circuitry for stereo output phase expansion, a joystick interface with timer, serial ports for DSP and I^{2}S (2). The MODIO drivers use CPU resources to implement the flow of high-speed fax, data, and voice (with Echo Cancellation) while simultaneously handling audio signals. The AD1821 operates from a +5-V supply, is housed in a 100-lead PQFP. Price (10,000 per month) is $18 ($15 modem only).

Faxcode* 2252 or Circle 21 ▶

DDS with On-Chip D/A
AD9832 is complete, for 25-MHz clock, has 10-bit DAC

The AD9832 is a low-cost, complete direct digital synthesizer (DDS) on a chip, with 25-MHz clock speed and 10-bit resolution. It includes a phase accumulator, sine lookup table, and on-chip D/A converter to generate an output sine wave with an SFDR of 72 dBc. On-chip frequency and phase registers can be used to perform modulation, such as FSK, PSK, and QPSK. Frequency accuracy can be controlled to 1 part in 4×10^9. A serial interface is provided for loading settings and modulation signals.

Typical applications include DDS tuning and digital demodulation. Housed in a 16-pin TSSOP, it operates with a 3- or 5-V single supply, consuming 45 mW. A power-down capability (3 & 5 mW residual power with 3- & 5-V supplies) aids power conservation in battery-powered operations. Operation is from -40 to $+85°C$. Price in 1000s is $5.00.

Faxcode* 2210 or Circle 22 ▶

RS-485 Transceivers
Full-duplex ADM488, 489 are in 8-pin μSOIC, TSSOP-14

The ADM488 and ADM489 are low-power full-duplex (receive and transmit) differential line transceivers suitable for communication on multipoint bus transmission lines. Like other industry-standard devices, they meet EIA Standards RS-485 and RS-422, but with less quiescent current (37-μA I_{DD}), greater supply tolerance (10%), and smaller packaging (TSSOP: ADM489) than is typically available in comparable devices.

In addition, their 2-kV EFT protection meets IEC1000-4-4, and EMI immunity meets IEC1000-4-3. They are short-circuit protected and have controlled slew rate for low EMI. The **ADM489** is available in 14-pin DIP and SOIC, as well as 16-pin TSSOP; the **ADM488** is in 8-lead plastic DIP and narrow-body SOIC. Supply voltage is +5 V; operation is from -40 to $+85°C$. Price (1000s) is $1.10.

Faxcodes* 2179 or Circle 23 ▶

μP Supervisory IC
ADM1232 provides manual or Vcc-out-of-tolerance Reset

The ADM1232 is a microprocessor supervisory circuit with existing second sources. It can monitor μP supply voltage tolerance (selectable –5%, –10%); it can detect an external interrupt; and its watchdog timer determines (with selectable time delay) when the μP has locked up. The device can then respond to any of these stimuli with a direct or complementary RESET signal.

A universally required component of digital systems, typical applications of the ADM1232 are in microprocessor systems, portable equipment, computers, controllers, intelligent instruments, automotive systems, and for protection against μP failure. The ADM1232 operates at +5 V, with 500-μA maximum quiescent current drain. It is available for –40 to +85°C in 8 lead PDIP, narrow SOIC, and microSOIC, as well as 16-lead wide SOIC. Price (1000s) is $0.90.

Faxcode* 2182 or Circle 24 ▶

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Signal Processing, Regulation, & Control

Low-Cost SHARCs

ADSP-21061 for 5 V
ADSP-21061L for 3.3 V

The ADSP-21061 and ADSP-21061L are fast (up to 50 MIPS/150MFLOPS), low-cost versions of the SHARC® (super Harvard architecture computer) 32-bit floating-point processor family. Code-compatible to their kin, they differ mainly in memory (1 Mbit of on-chip SRAM vs. up to 4 Mbits), with 6 instead of 10 DMA channels and no link ports (nevertheless, up to 6 SHARCs can be used in cluster multiprocessing). They are supported by SHARC EZ-Kit Lite low-cost evaluation board and development tools—*including a C compiler.* Applications include prosumer audio, communications, imaging, industrial.

Housed in a 240-lead metric PQFP, for 0 to +85°C, peak performances of 100/120/150 MFLOPS are available at 33/40/50 MIPS. Prices in 1000s for the ADSP-21061 and L start at $64/$39. The EZ-Kit Lite is $179.

Circle 26, 25 ADSP-21061, -21061L ▷

CCD/CIS Processor

10-bit AD9805 is complete
1-chip CCD imaging front end

The AD9805, like the pin-compatible 12-bit AD9807 (*Analog Dialogue* 31-1, p. 19), is a complete single-chip analog front end (AFE) for converting outputs from CCD (charge-coupled device) and CIS (contact image sensor) modules to digital data. It requires no external active circuitry, just a few capacitors. Typical applications are in scanners and other CCD signal-processing applications, such as digital cameras.

It includes a 10-bit, 6-MSPS A/D converter, an integrated triple-correlated double sampler, programmable-gain amplifiers, pixel rate digital gain and offset adjustments, an internal voltage reference, and a μP-compatible control interface. It uses a 5-V supply (500 mW) and is compatible with 3.3- and 5-V digital I/O. Specified for 0 to +70°C, it is packaged in a 64-pin PQFP. Price (1000s) is $9.50

Faxcode* 2021 or Circle 27 ▷

CCD Processor

For electronic cameras: 10-
bit 18-MSPS full speed CDS

The AD9801 is a complete CCD signal processor developed for electronic cameras. It is well-suited for both video conferencing and consumer-level still camera applications. Its signal-processing chain comprises a high-speed (18-MSPS) correlated double sampler (CDS), a low noise, wideband variable-gain amplifier (0 to 31.5 dB, linear in dB), and a 10-bit, 18-MSPS A/D converter (±0.5-LSB DNL, no-missing-codes guaranteed). Also included are an on-chip voltage reference and the required clamping circuitry for simple ac coupling. Digital output control is 3-state.

The AD9801 operates from a single +3-V supply and typically consumes 185 mW (15 mW in power-down mode). It is packaged in space-saving 48-pin TQFP and specified for an operating temperature range of 0 to +70°C. Price is $8.50 (1000s).

Faxcode* 2118 or Circle 28 ▷

AC Motor Controller

Single-chip ADMC330 joins
DSP & MC peripherals

The ADMC330 is a low-cost single-chip controller comprising a 20-MIPS ADSP-2171 core (with on-chip RAM and ROM) and the necessary motor-control peripherals, including a 3-phase center-based PWM generator, a seven-channel (3 independent, 4×1 multiplexed) slope/comparator ADC, 8 bits of digital I/O, etc. It is used for ac motor control in domestic appliances, industrial machinery, electric vehicles, and wherever else electric motors must be controlled.

On a single chip, the DSP performs all the necessary calculations required for closed-, open-, or servoloop motor control; and the motor-control peripherals initiate the appropriate PWM waveforms—all with little external circuitry and software overhead. The ADMC330, in an 80-lead TQFP, uses +5 V, operates from –40 to +85°C. Price is $13.60 (1000s). An evaluation kit is $395.

Faxcode* 2126 or Circle 29 ▷

Regulator Controller

ADP3310 is a low-noise high
precision LDO in 8-pin SOIC

The ADP3310 is a precision voltage-regulator controller that can be used with an external power PMOS device, such as the NDP6020P, to form a two-chip low-dropout linear regulator with only 70 mV of dropout voltage at 1 A. Its low headroom, low quiescent current (800 μA), and low shutdown current (1 μA) help prolong battery life in battery-powered systems. Its accuracy spec is ±1.5% over line, load, and temperature. Handling up to 10 A of current, it is stable with 10-μF output capacitance.

Protection includes an internal gate-to source clamp, and current limiting, with foldback. Operating voltage is from +2.5 to +15 V. It is packaged in an 8-lead SOIC and has a –40 to +85°C ambient temperature range. 4 fixed output options are available: 1.8, 3, 3.3, & 5 V. Price (1000s) is $0.94.

Faxcode* 2120 or Circle 30 ▷

LD Regulators

50/200-mA ADP3300/3303
use any type quality capacitor

The ADP3300 and ADP3303 are anyCAP™ low-dropout linear regulators with wide input voltage range (3.2 to 12 V), high accuracy (±0.8% @ 25°C), and low dropout voltage. The 50-mA **ADP3300**, with dropout voltage of 80 mV, is housed in a tiny SOT23-6 package; and the 200-mA **ADP3303** (180 mV) inhabits an efficient thermally enhanced SO-8 package. Both devices offer a range of optional regulated output voltages: 2.7, 3.0, 3.2, 3.3. and 5.0 V.

Both devices are stable with a wide range of capacitor values (≥0.47 μF), types, and ESRs (anyCAP™). Both have low noise, dropout detector, current- and thermal limiting, and 1-μA shutdown current. The ADP3300 operates from –40 to +85°C, the ADP3303 from–20 to+85°C ambient. Their respective prices are $0.86 and $1.14 in 1000s.

Faxcode* 2042, 2043 or Circle 31, 32 ▷

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Ask The Applications Engineer—26

by Mary McCarthy & Anthony Collins

SWITCHES AND MULTIPLEXERS

Q. *Analog Devices doesn't specify the bandwidth of its ADG series switches and multiplexers. Is there a reason?*

A. The ADG series switches and multiplexers have very high input bandwidths, in the hundreds of megahertz. However, the bandwidth specification by itself is not very meaningful, because at these high frequencies, the off-isolation and crosstalk will be significantly degraded. For example, at 1 MHz, a switch typically has off-isolation of 70 dB and crosstalk of –85 dB. Both off-isolation and crosstalk degrade by 20 dB per decade. This means that at 10 MHz, the off-isolation is reduced to 50 dB and the crosstalk increases to –65 dB. At 100 MHz, the off-isolation will be down to 30 dB while the crosstalk will have increased to –45 dB. So it is not sufficient to consider bandwidth alone—the off-isolation and crosstalk must be considered to determine if the application can tolerate the degradation of these specifications at the required high frequency.

Q. *Which switches and multiplexers can be operated with power supplies less than those specified in the data sheet?*

A. All of the ADG series switches and multiplexers operate with power supplies down to +5 V or ±5 V. The specifications affected by power-supply voltage are timing, on resistance, supply current and leakage current. Lowering power supply voltage reduces power supply current and leakage current. For example, the ADG411's $I_{S(OFF)}$ and $I_{D(OFF)}$ are ±20 nA, and $I_{D(ON)}$ is ±40 nA, at +125°C with a ±15-V power supply. When the supply voltage is reduced to ±5 V, $I_{S(OFF)}$ and $I_{D(OFF)}$ drop to ±2.5 nA, while $I_{D(ON)}$ is reduced to ±5 nA at +125°C. The supply currents, I_{DD}, I_{SS} and I_L, are 5 µA maximum at +125°C with a ±15-V power supply. When a ±5-V power supply is used, the supply currents are reduced to 1 µA maximum. The on-resistance and timing increase as the power supply is reduced. The Figures below show how the timing and on-resistance of the ADG408 vary as a function of power supply voltage.
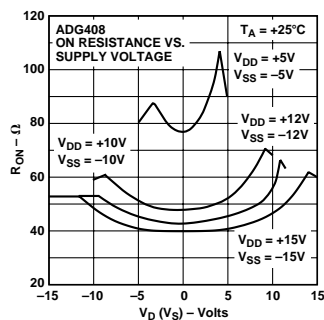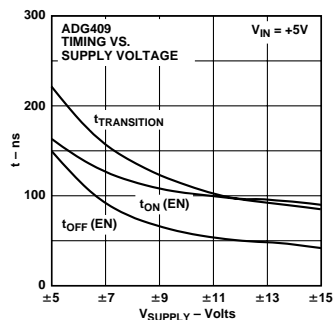
Figure 1. On-Resistance vs Power Supply.

Figure 2. Timing vs Power Supply.

Q. *Some of the ADG series switches are fabricated on the DI process. What is it?*

A. DI is short for dielectric isolation. On the DI process, an insulating layer (trench) is placed between the NMOS and PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in standard switches, are eliminated, resulting in a completely latchup-proof switch. In junction isolation (no trench used), the N and P wells of the PMOS and NMOS transistors form a diode which is reverse-biased in normal operation. However, during overvoltage or power-off conditions, when the analog input exceeds the power supplies, the diode is forward biased, forming a silicon controlled rectifier (SCR)-like circuit with the two transistors, causing the current to be amplified significantly, leading eventually to latch up. This diode doesn't exist in dielectrically isolated switches, making the part latchup proof.
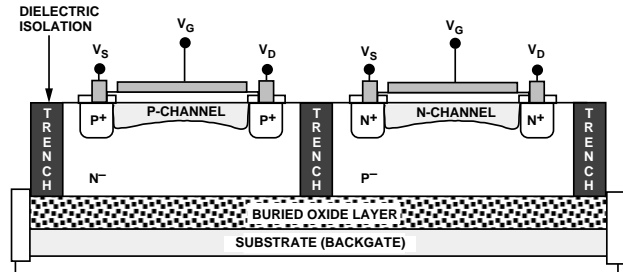
Figure 3. Dielectric Isolation.

Q. *How do the fault-protected multiplexers and channel protectors work?*

A. A channel of a fault-protected multiplexer or channel protector consists of two NMOS and two PMOS transistors. One of the PMOS transistors does not lie in the direct signal path but, is used to connect the source of the second PMOS to its backgate. This has the effect of lowering the threshold voltage, which increases the input signal range for normal operation. The source and backgate of the NMOS devices are connected for the same reason. During normal operation, the fault-protected parts operate as a standard multiplexer. When a fault condition occurs on the input to a channel, this means that the input has exceeded some threshold voltage which is set by the supply rail voltages. The threshold voltages are related to the supply rails as follows: for a positive overvoltage, the threshold voltage is given by $V_{DD} - V_{TN}$ where V_{TN} is the threshold voltage of the NMOS transistor (typically 1.5 V). For a negative overvoltage, the threshold voltage is given by $V_{SS} - V_{TP}$, where V_{TP} is the threshold voltage of the PMOS device (typically 2 V). When the input voltage exceeds these threshold voltages, with no load on the channel, the output of the channel is clamped at the threshold voltage.

Q. *How do the parts operate when an overvoltage exists?*

A. The next two figures show the operating conditions of the signal path transistors during overvoltage conditions. This one demonstrates how the series N, P and N transistors operate when a *positive* overvoltage is applied to the channel. The first NMOS transistor goes into saturation mode as the voltage on its drain exceeds ($V_{DD} - V_{TN}$). The potential at the source of the NMOS device is equal to ($V_{DD} - V_{TN}$). The other MOS devices are in a non-saturated mode of operation.
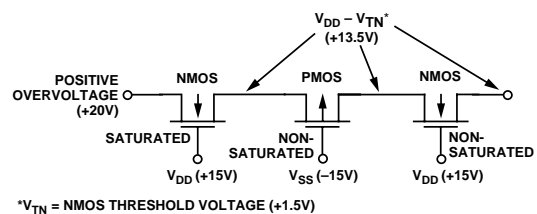
Figure 4. Positive Overvoltage on the Channel.

When a *negative* overvoltage is applied to a channel, the PMOS transistor enters a saturated mode of operation as the drain voltage exceeds ($V_{SS} - V_{TP}$). As with a positive overvoltage, the other MOS devices are non-saturated.
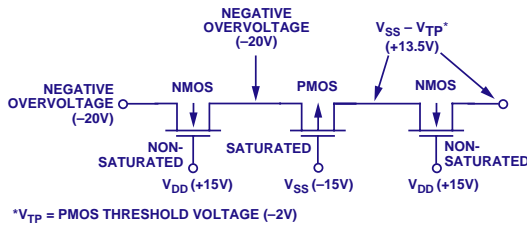

Figure 5. Negative Overvoltage on the Channel.

Q. *How does loading affect the clamping voltage?*

A. When the channel is loaded, the channel output will clamp at a value of voltage between the thresholds. For example, with a load of 1 kΩ, V_{DD} = 15 V, and a positive overvoltage, the output will clamp at $V_{DD} - V_{TN} - \Delta V$, where ΔV is due to the IR voltage drop across the channels of the non-saturated MOS devices. In the example shown below the voltage at the output of the clamped NMOS is 13.5 V. The on-resistance of the two remaining MOS devices is typically 100 Ω. Therefore, the current is 13.5 V/(1 kΩ + 100 Ω) = 12.27 mA. This produces a voltage drop of 1.2 V across the NMOS and PMOS resulting in a clamp voltage of 12.3 V. The current during a fault condition is determined by the load on the output, i.e., V_{CLAMP}/R_L.
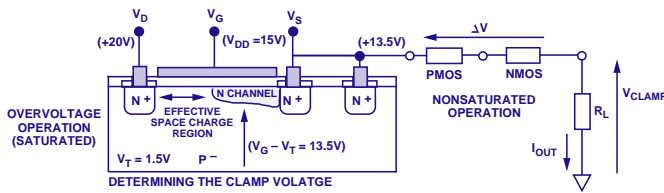

Figure 6. Determining the clamping point.

Q. *Do the fault-protected multiplexers and channel protectors function when the power supply is absent.*

A. Yes. These devices remain functional when the supply rails are down or momentarily disconnected. When V_{DD} and V_{SS} equal 0 V, all the transistors are off, as shown, and the current is limited to sub nanoampere levels.
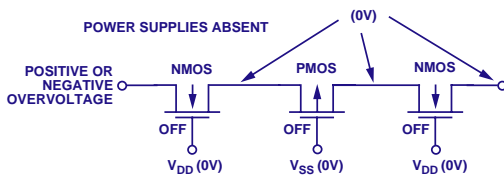

Figure 7. Power Supplies Absent.

Q. *What is "charge injection"?*

A. Charge injection in analog switches and multiplexers is a level change caused by stray capacitance associated with the NMOS and PMOS transistors that make up the analog switch. The Figure below models the structure of an analog switch and the

stray capacitance associated with such an implementation. The structure basically consists of an NMOS and PMOS device in parallel. This arrangement produces the familiar "bathtub" resistance profile for bipolar input signals. The equivalent circuit shows the main parasitic capacitances that contribute to the charge injection effect, C_{GDN} (NMOS gate to drain) and C_{GDP} (PMOS gate to drain). The gate-drain capacitance associated with the PMOS device is about twice that of the NMOS device, because for both devices to have the same *on*-resistance, the PMOS device has about twice the area of the NMOS. Hence the associated stray capacitance is approximately twice that of the NMOS device for typical switches found in the marketplace.
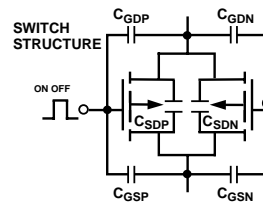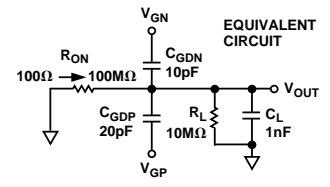

figure 8   *figure 9*

Figure 8. CMOS Switch Structure showing parasitic capacitance.
Figure 9. Equivalent circuit showing the main parasitics which contribute to charge injection.

When the switch is turned on, a positive voltage is applied to the gate of the NMOS and a negative voltage is applied to the gate of the PMOS. Because the stray gate-to-drain capacitances are mismatched, unequal amounts of positive and negative charge are injected onto the drain. The result is a removal of charge from the output of the switch, manifested as a negative-going voltage spike. Because the analog switch is now turned on this negative charge is quickly discharged through the on resistance of the switch (100 Ω). This can be seen in the simulation plot at 5 μs. Then when the switch is turned off, a negative voltage is applied to the gate of the NMOS and a positive voltage is applied to the gate of the PMOS. The result is charge added to the output of the switch. Because the analog switch is now off, the discharge path for this injected positive charge is a high impedance (100 MΩ). The result is that the load capacitance stores this charge until the switch is turned on again. The simulation plot clearly shows this with the voltage on C_L (as a result of charge injection) remaining constant at 170 mV until the switch is again turned on at 25 μs. At this point an equivalent amount of negative charge is injected onto the output, reducing the voltage on C_L to 0 V. At 35 μs the switch is turned on again and the process continues in this cyclic fashion.
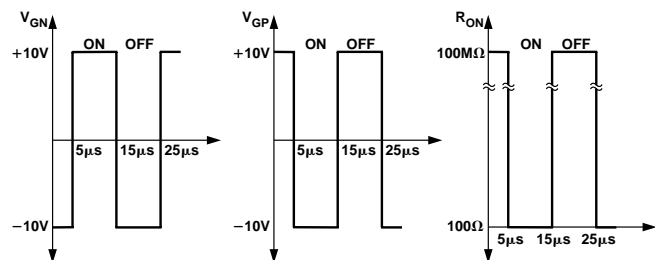

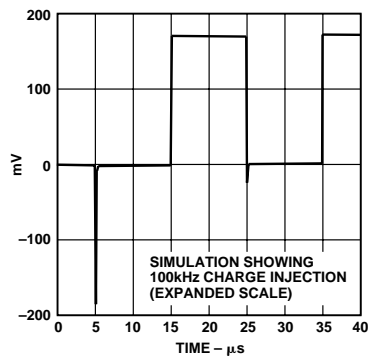Figure 10. Timing used for simulation in Figure 11.

Figure 11. Output of simulation to show the effect of charge injection switching at 100 kHz.

At lower switching frequencies and load resistance, the switch output would contain both positive and negative glitches as the injected charge leaks away before the next switch transition.
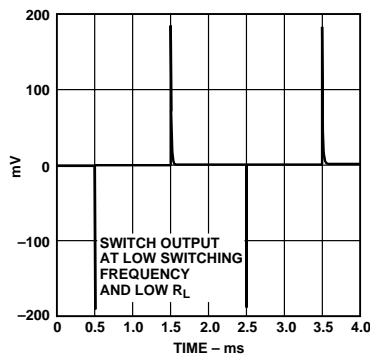

Figure 12. Switch output at low switching frequencies and low resistive loads.

Q. *What can be done to improve the charge injection performance of an analog switch?*

A. As noted above, the charge injection effect is caused by a mismatch in the parasitic gate-to-drain capacitance of the NMOS and PMOS devices. So if these parasitics can be matched there will be little if any charge injection effect. This is precisely what is done in Analog Devices CMOS switches and multiplexers. The matching is accomplished by introducing a dummy capacitor between the gate and drain of the NMOS device.
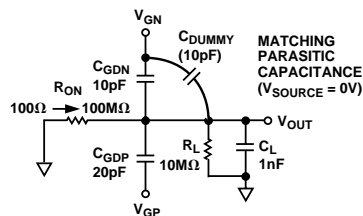

Figure 13. Matching parasitics at V_{SOURCE} = 0 V (ground).

Unfortunately the matching is only accomplished under a specific set of conditions, i.e., when the voltage on the Source of both devices is 0 V. The reason for this is that the parasitic capacitances, C_{GDN} and C_{GDP}, are not constant; they vary with the Source voltage. When the Source voltage of the NMOS and PMOS is varied, their channel depths vary, and with them, C_{GDN} and C_{GDP}. As a consequence of this matching at V_{SOURCE} = 0 V the charge injection effect will be noticeable for other values of V_{SOURCE}.

NOTE: Charge injection is usually specified on the data sheet under these matched conditions, i.e., V_{SOURCE} = 0 V. Under these conditions, the charge injection of most switches is usually quite good in the order of 2 to 3 pC max. However the charge injection will increase for other values of V_{SOURCE}, to an extent depending on the individual switch. Many data sheets will show a graph of charge injection as a function of Source voltage.

Q. *How do I minimize these effects in my application?*

A. The effect of charge injection is a voltage glitch on the output of the switch due to the injection of a fixed amount of charge. The glitch amplitude is a function of the load capacitance on the switch output and also the turn on and turn off times of the switch. The larger the load capacitance, the smaller will be the voltage glitch on the output, i.e., $Q = C \times V$, or $V = Q/C$, and Q is fixed. Naturally, it may not always be possible to increase the load capacitance, because it would reduce the bandwidth of the channel. However, for audio applications, increasing the load capacitance is an effective means of reducing those unwanted "pops" and "clicks".

Choosing a switch with a slow turn on and turn off time is also an effective means of reducing the glitch amplitude on the switch output. The same fixed amount of charge is injected over a longer time period and hence has a longer time period in which to leak away. The result is a wider glitch but much reduced in amplitude. This technique is used quite effectively in some of the audio switch products, such as the SSM-2402/SSM-2412, where the turn on time is designed to be of the order of 10 ms.

Another point worth mentioning is that the charge injection performance is directly related to the *on*-resistance of the switch. In general the lower the R_{ON}, the poorer the charge injection performance. The reason for this is purely due to the associated geometry, because R_{ON} is decreased by increasing the area of the NMOS and PMOS devices, thus increasing C_{GDN} and C_{GDP}. So trading off R_{ON} for reduced charge injection may also be an option in many applications.

Q. *How can I evaluate the charge injection performance of an analog switch or multiplexer?*

A. The most efficient way to evaluate a switch's charge injection performance is to use a setup similar to the one shown below. By turning the switch on and off at a relatively high frequency (>10 kHz) and observing the switch output on an oscilloscope (using a high impedance probe), a trace similar to that shown in Figure 11 will be observed. The amount of charge injected into the load is given by $\Delta V_{OUT} \times C_L$. Where ΔV_{OUT} is the output pulse amplitude.
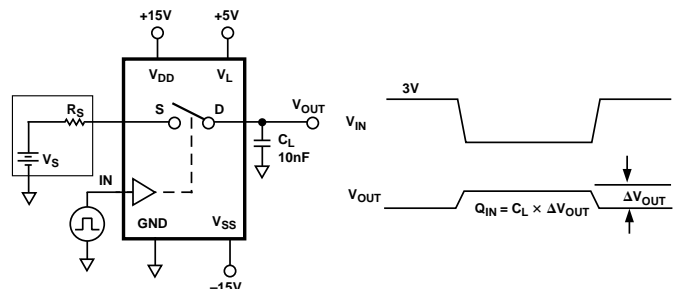

Figure 14. Evaluating the charge injection performance of an analog Switch or Multiplexer.

MORE AUTHORS [*Continued from page 2*]

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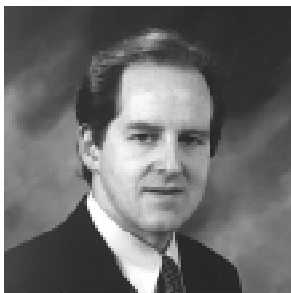
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NEW PATENTS [*not available from Analog Devices*]

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